

AO 120 (Rev. 2/99)

TO: <b>Mail Stop 8</b> <b>Director of the U.S. Patent &amp; Trademark Office</b> <b>P.O. Box 1450</b> <b>Alexandria, VA 22313-1450</b>	<b>REPORT ON THE</b> <b>FILING OR DETERMINATION OF AN</b> <b>ACTION REGARDING A PATENT OR</b> <b>TRADEMARK</b>
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In Compliance with 35 § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been  
filed in the U.S. District Court Northern District of California on the following ☒ Patents or ☐ Trademarks:

DOCKET NO. <b>CV 09-05235 EMC</b>	DATE FILED <b>11/4/09</b>	U.S. DISTRICT COURT <b>Northern District of California, San Francisco Division</b>
PLAINTIFF <b>POWER INTEGRATIONS INC.</b>		DEFENDANT <b>FAIRCHILD SEMICONDUCTOR</b>
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 <b>6,351,398</b>		
2		
3		
4		
5		

In the above—entitled case, the following patent(s) have been included:

DATE INCLUDED	INCLUDED BY <input type="checkbox"/> Amendment <input type="checkbox"/> Answer <input type="checkbox"/> Cross Bill <input type="checkbox"/> Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
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CLERK <b>Richard W. Wicking</b>	(BY) DEPUTY CLERK <b>Gloria Acevedo</b>	DATE <b>November 6, 2009</b>
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Copy 1—Upon initiation of action, mail this copy to Commissioner Copy 3—Upon termination of action, mail this copy to Commissioner  
Copy 2—Upon filing document adding patent(s), mail this copy to Commissioner Copy 4—Case file copy

1 Certificate No. 6,212,079 C1, confirming the patentability of many of the '079 patent  
2 over SG's challenges. A true and correct copy of the '079 Reexamination Certificate is attached  
3 hereto as Exhibit F.

4 39. After the USPTO confirmed the validity of claims in all of the patents previously  
5 asserted against SG, Power Integrations contacted Defendants regarding their continued  
6 infringement in a letter dated August 10, 2009. Despite the USPTO's confirmation of the validity  
7 of the '079 patent, Defendants have refused to agree to stop infringing the '079 patent.

8 40. Defendants have been and are now infringing, inducing infringement, and  
9 contributing to the infringement of the '079 patent in this District and elsewhere by making, using,  
10 selling, offering to sell, and/or importing devices, including power supply controller integrated  
11 circuit devices, covered by one or more claims of the reexamined '079 patent, and/or contributing to  
12 or inducing the same by third-parties, all to the injury of Power Integrations. In particular,  
13 Defendants' power supply controller products that include what Defendants characterize as "Green-  
14 Mode" functionality, or other substantially similar functionality, infringe Power Integrations' '079  
15 patent.

16 41. Defendants' acts of infringement have injured and damaged Power Integrations.

17 42. Defendants' acts of infringement have been, and continue to be, willful so as to  
18 warrant the enhancement of damages awarded as a result of their infringement. In particular,  
19 despite Power Integrations' prior notice of the infringement as early as 2004, despite the '079 patent  
20 emerging from reexamination, and despite Power Integrations' renewed notice to Defendants of  
21 their infringement, Defendants have continued to infringe the '079 patent and have failed to commit  
22 to ceasing all infringement of the '079 patent.

23 43. Defendants' infringement has caused irreparable injury to Power Integrations and  
24 will continue to cause irreparable injury until Defendants are enjoined from further infringement by  
25 this Court.

26 **PRAYER FOR RELIEF**

27 WHEREFORE, Plaintiff requests the following relief:

28 (a) judgment that Defendants infringe the '398 patent and that the patent is valid;

- 1 (b) judgment that Defendants infringe the '908 patent and that the patent is valid;
- 2 (c) judgment that Defendants infringe the '079 patent and that the patent is valid;
- 3 (d) a permanent injunction preventing Defendants and their officers, directors, agents,
- 4 servants, employees, attorneys, licensees, successors, assigns, and customers, and those in active
- 5 concert or participation with any of them, from making, using, offering to sell, or selling in the
- 6 United States or importing into the United States any devices that infringe any claim of the '398,
- 7 '908, or '079 patents, or contributing to or inducing the same by others;
- 8 (e) judgment against Defendants for money damages sufficient to compensate Power
- 9 Integrations for Defendants' infringement of the '398, '908, and '079 patents in an amount to be
- 10 determined at trial;
- 11 (f) that such money judgment be trebled as a result of the willful nature of Defendants'
- 12 infringement;
- 13 (g) an accounting for infringing sales not presented at trial and an award by the Court of
- 14 additional damages for any such infringing sales;
- 15 (h) costs and reasonable attorneys' fees incurred in connection with this action pursuant
- 16 to 35 U.S.C. § 285; and
- 17 (i) such other and further relief as the Court finds just and proper.

18 A JURY TRIAL IS DEMANDED BY PLAINTIFF.

19

20 Dated: November 4, 2009

FISH & RICHARDSON P.C.

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22 By:   
Howard G. Pollack

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24 Attorneys for Plaintiff

25 POWER INTEGRATIONS, INC.

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US006351398B1

(12) **United States Patent**  
Balakrishnan et al.

(10) **Patent No.:** US 6,351,398 B1  
(45) **Date of Patent:** Feb. 26, 2002

(54) **METHOD AND APPARATUS PROVIDING A MULTI-FUNCTION TERMINAL FOR A POWER SUPPLY CONTROLLER**

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5,959,851 A 9/1999 Shutts ..... 363/21  
5,982,639 A 11/1999 Balakrishnan ..... 363/21

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\* cited by examiner

(73) **Assignee:** Power Integrations, Inc., San Jose, CA (US)

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(74) *Attorney, Agent, or Firm*—Blakely Sokoloff Taylor & Zafman, LLP

(\*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** 09/697,870

(22) **Filed:** Oct. 26, 2000

**Related U.S. Application Data**

(62) Division of application No. 09/405,209, filed on Sep. 24, 1999.

(51) **Int. Cl.** <sup>7</sup> ..... H02H 7/122

(52) **U.S. Cl.** ..... 363/56.03; 363/49; 363/16

(58) **Field of Search** ..... 323/282, 284, 323/901, 908; 363/16, 20–21.18, 49, 50, 97, 131, 56.03, 56.01; 361/22

(56) **References Cited**

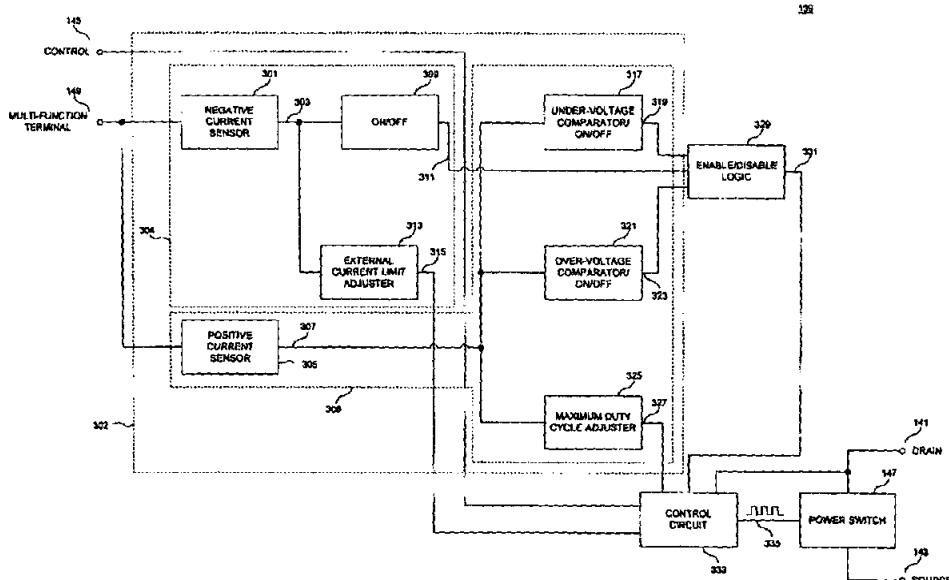
**U.S. PATENT DOCUMENTS**

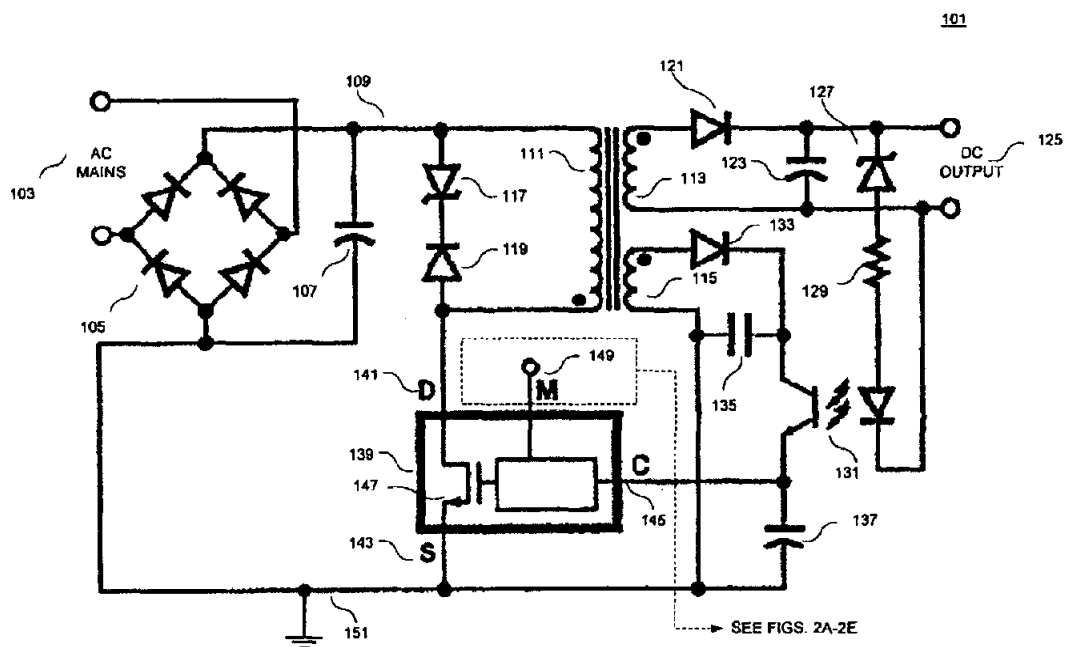
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(57) **ABSTRACT**

A power supply controller having a multi-function terminal. In one embodiment, a power supply controller for switched mode power supply includes a drain terminal, a source terminal, a control terminal and a multi-function terminal. The multi-function terminal may be configured in a plurality of ways providing any one or some of a plurality of functions including on/off control, external current limit adjustments, under-voltage detection, over-voltage detection and maximum duty cycle adjustment. The operation of the multi-function terminal varies depending on whether a positive or negative current flows through the multi-function terminal. A short-circuit to ground from the multi-function terminal enables the power supply controller. A short-circuit to a supply voltage from the multi-function terminal disables the power supply controller. The current limit of an internal power switch of the power supply controller may be adjusted by externally setting a negative current from the multi-function terminal. The multi-function terminal may also be coupled to the input DC line voltage of the power supply through a resistance to detect an under-voltage condition, an over-voltage condition and/or adjust the maximum duty cycle of power supply controller. Synchronization of the oscillator of the power supply controller may also be realized by switching the multi-function terminal to power or ground at the desired times.

**29 Claims, 13 Drawing Sheets**





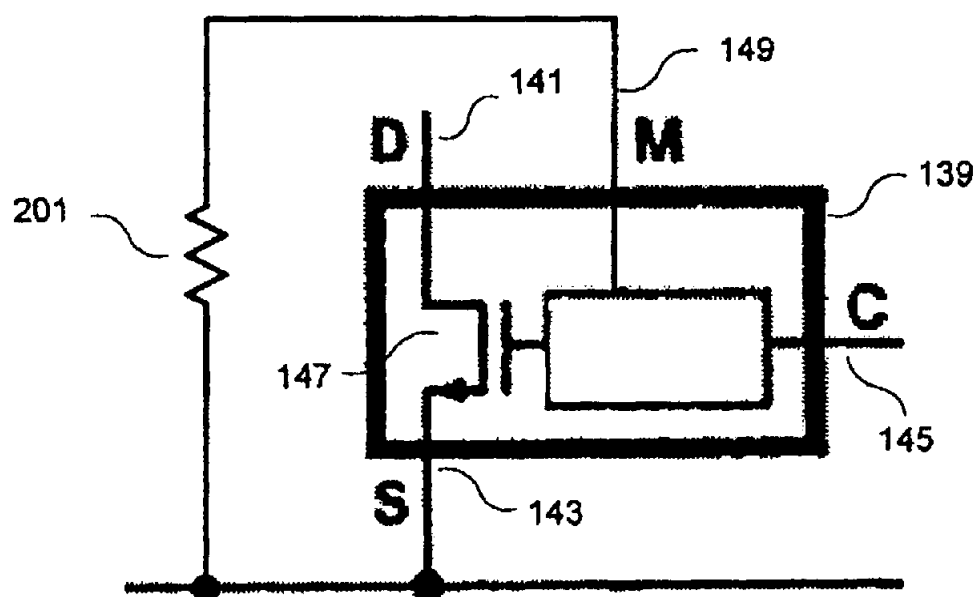


FIG. 2A

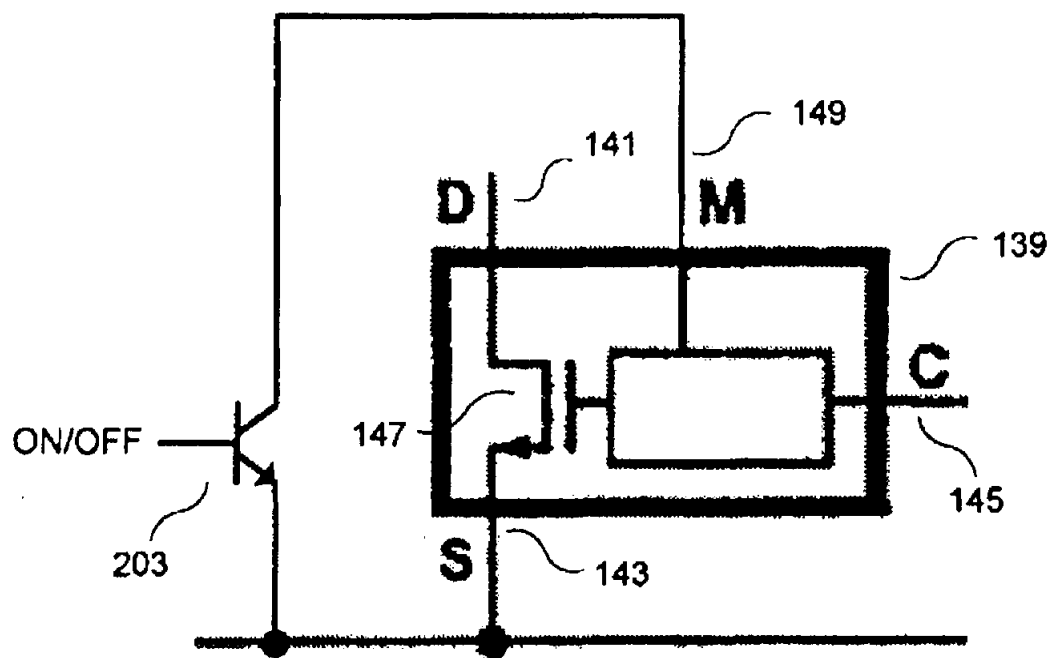


FIG. 2B



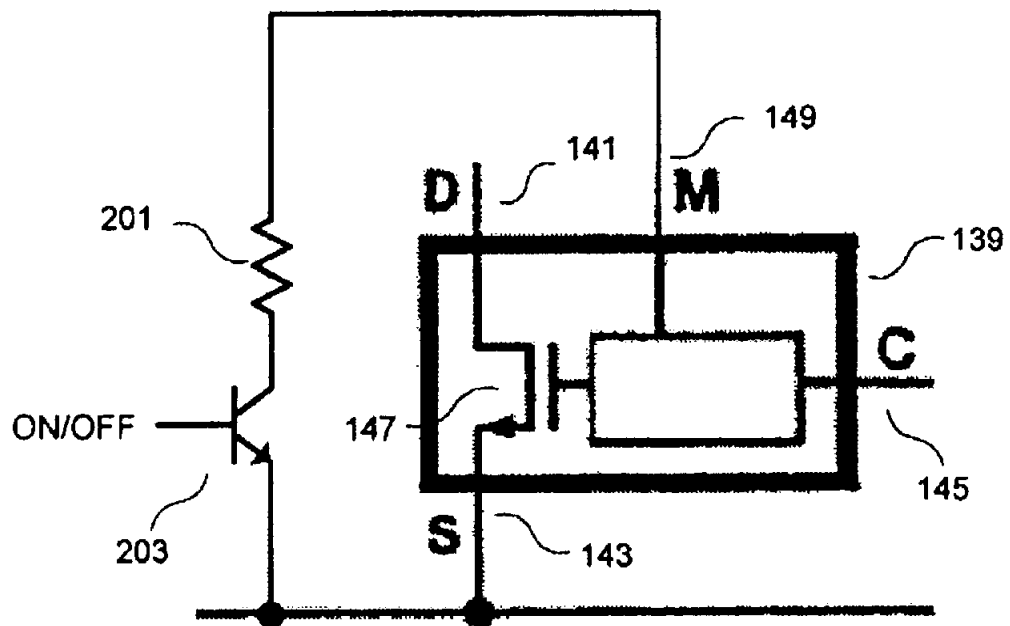


FIG. 2C

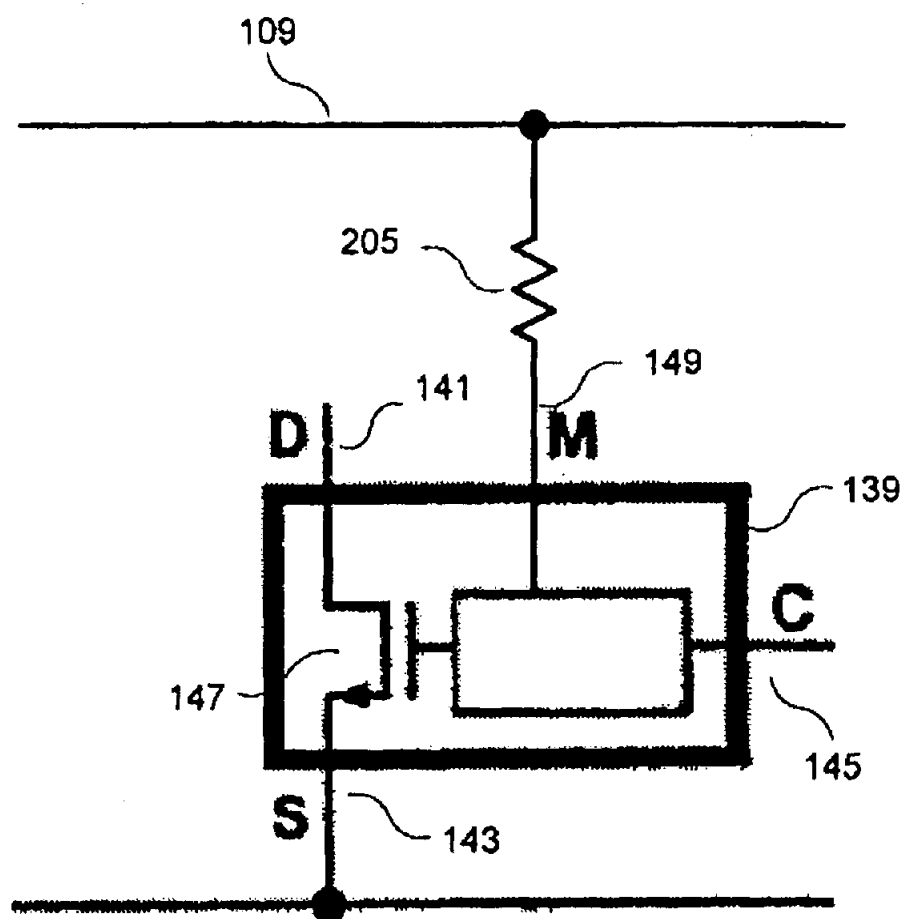


FIG. 2D

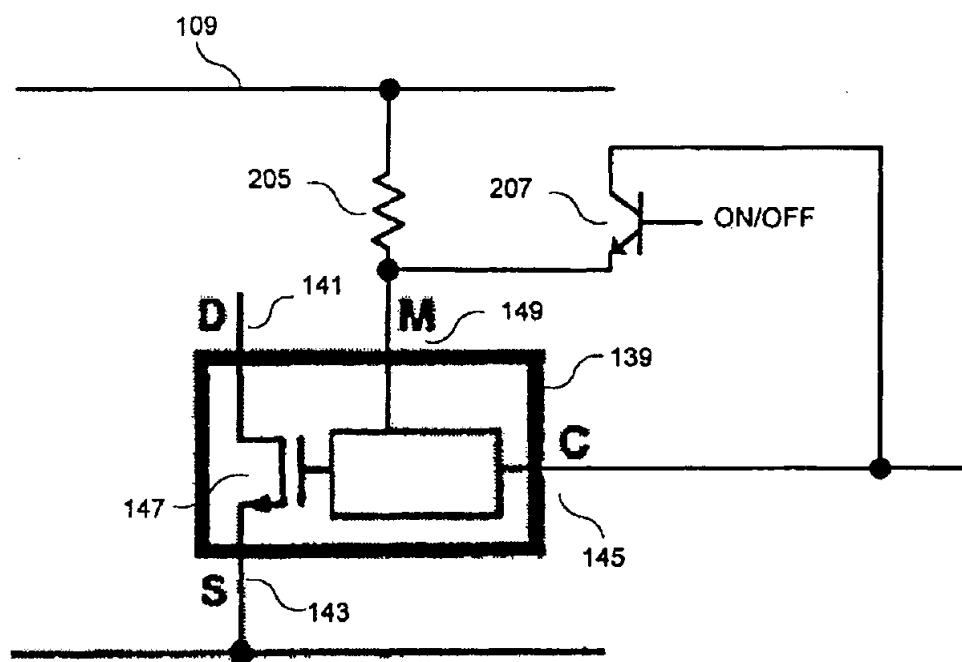


FIG. 2E

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ORIGINAL  
FILED

NOV - 4 2009

RICHARD W. WIEKING  
CLERK, U.S. DISTRICT COURT,  
NORTHERN DISTRICT OF CALIFORNIA

EMC

12 UNITED STATES DISTRICT COURT  
13 NORTHERN DISTRICT OF CALIFORNIA

14  
15 POWER INTEGRATIONS, INC., a Delaware  
corporation,

16  
17 Plaintiff,

18 v.

19 FAIRCHILD SEMICONDUCTOR  
20 INTERNATIONAL, INC., a Delaware  
corporation, FAIRCHILD SEMICONDUCTOR  
21 CORPORATION, a Delaware corporation, and  
22 SYSTEM GENERAL CORPORATION, a  
Taiwanese corporation,

23  
24 Defendants.

CV 09-00000

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COMPLAINT FOR PATENT  
INFRINGEMENT

DEMAND FOR JURY TRIAL

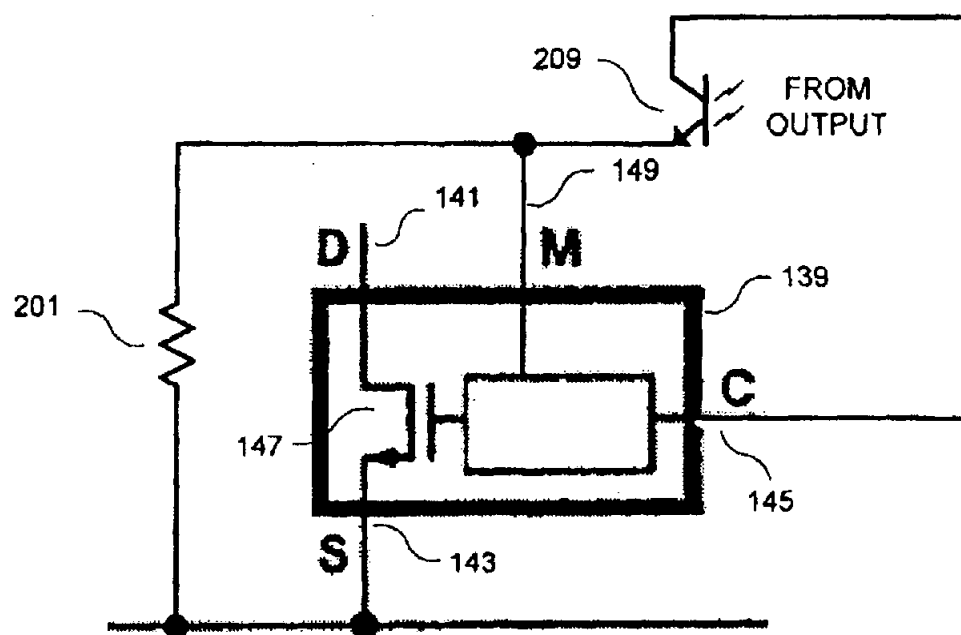


FIG. 2F

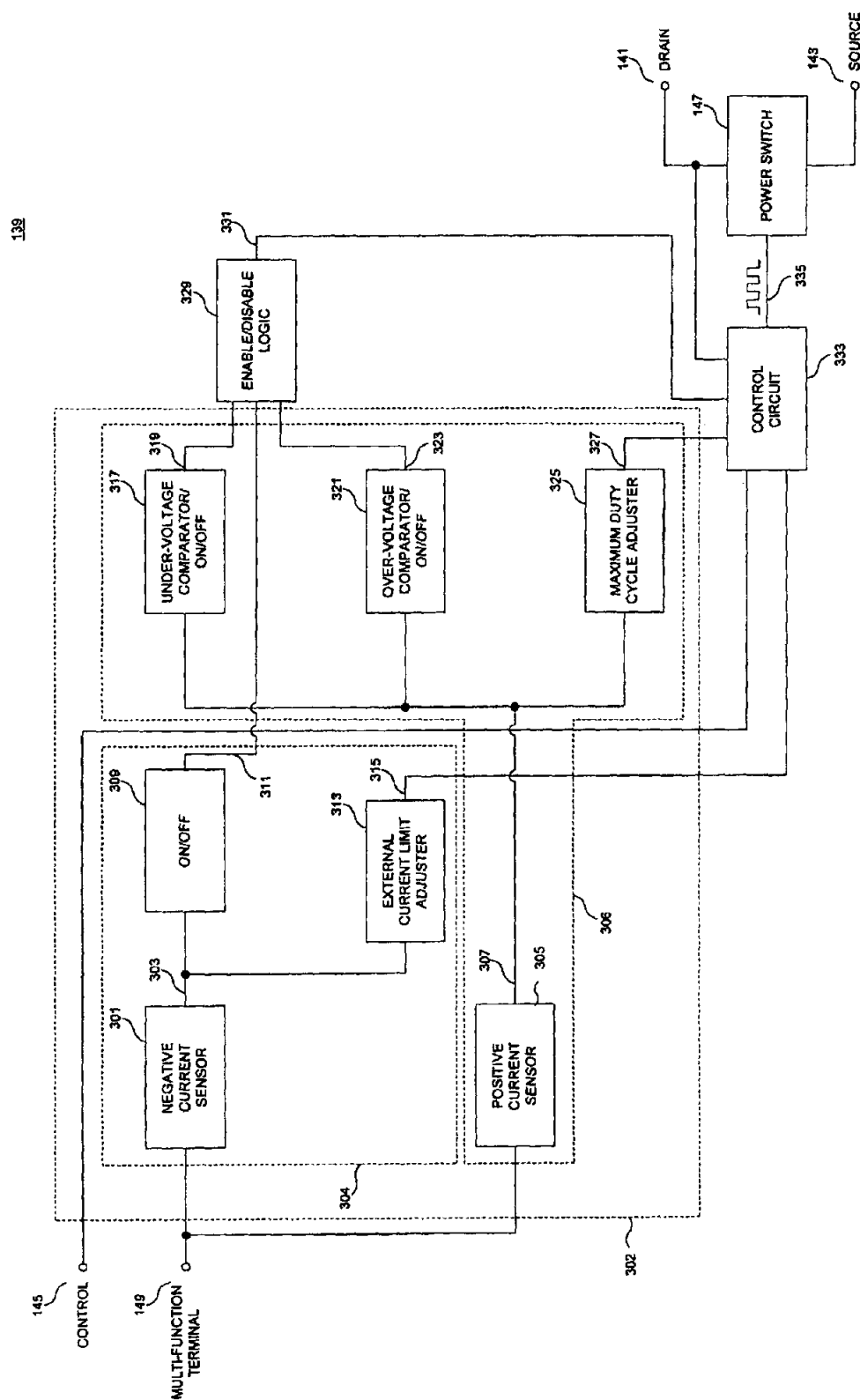


FIG. 3

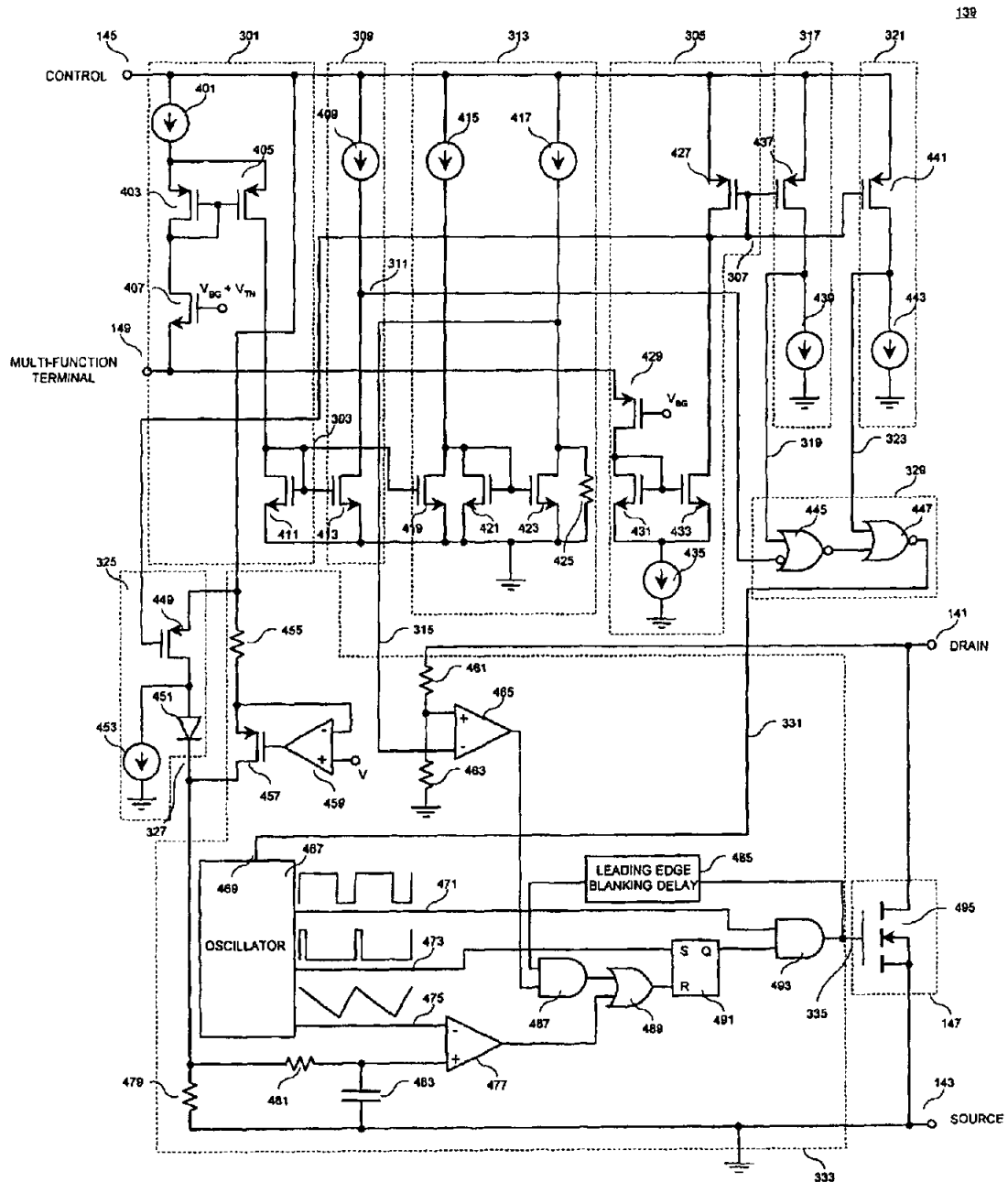


FIG. 4

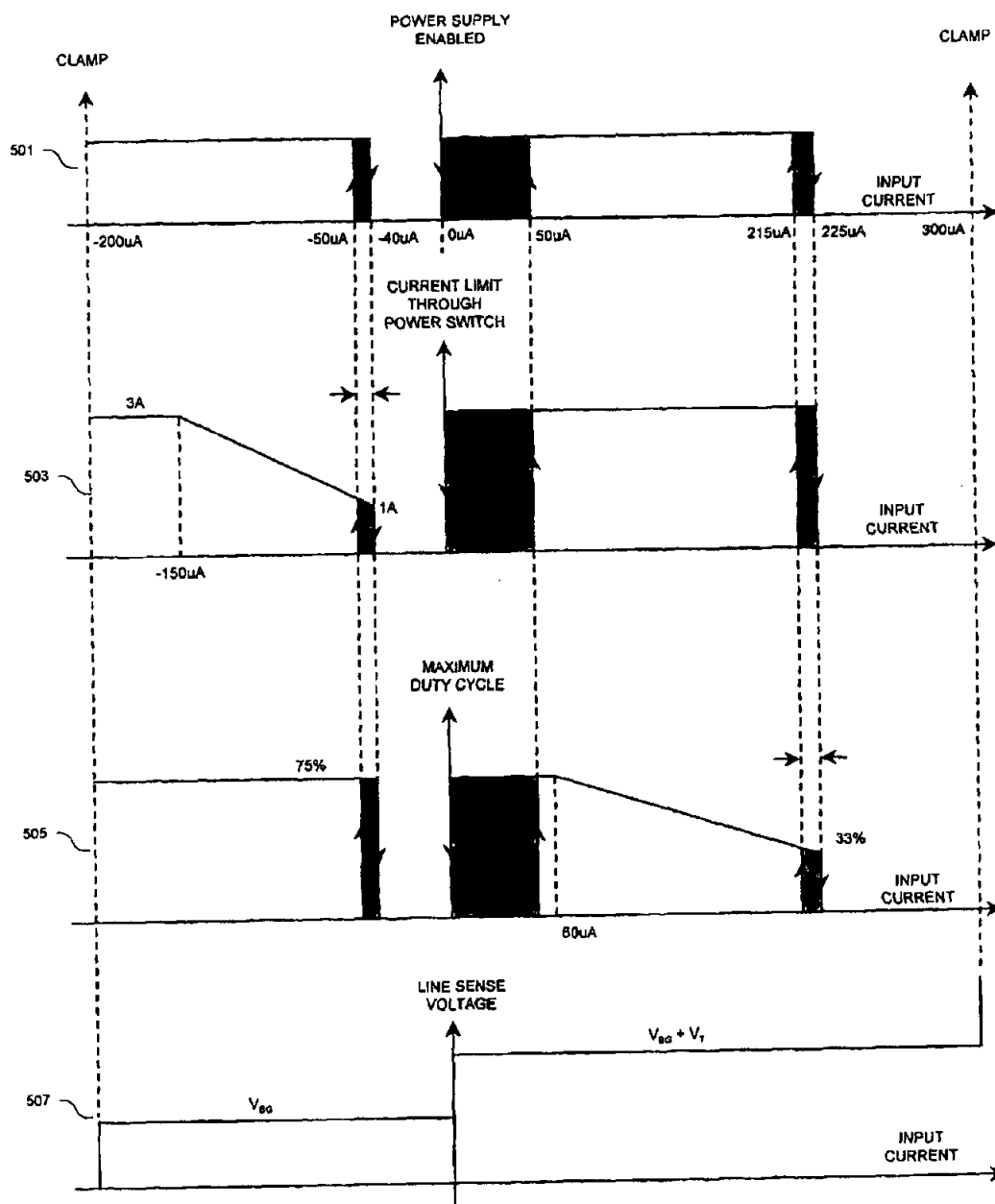


FIG. 5



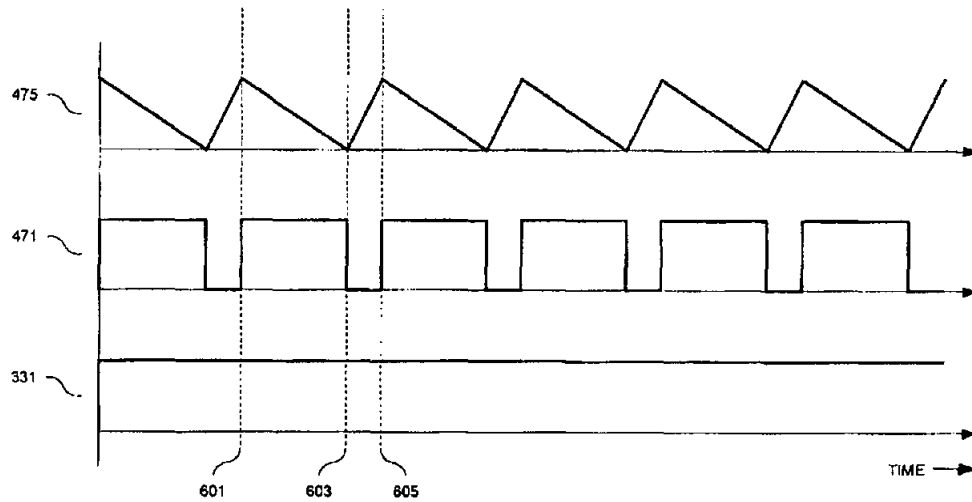


FIG. 6A

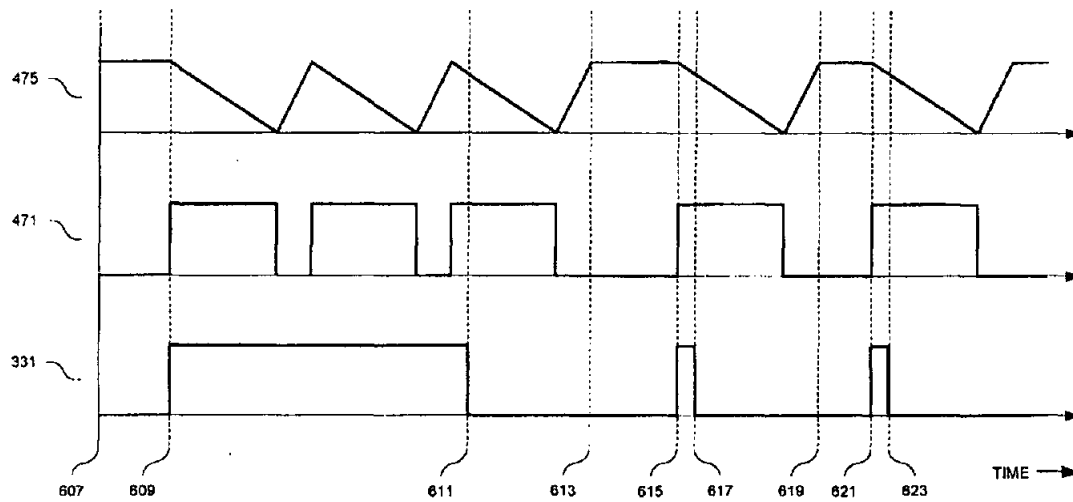


FIG. 6B

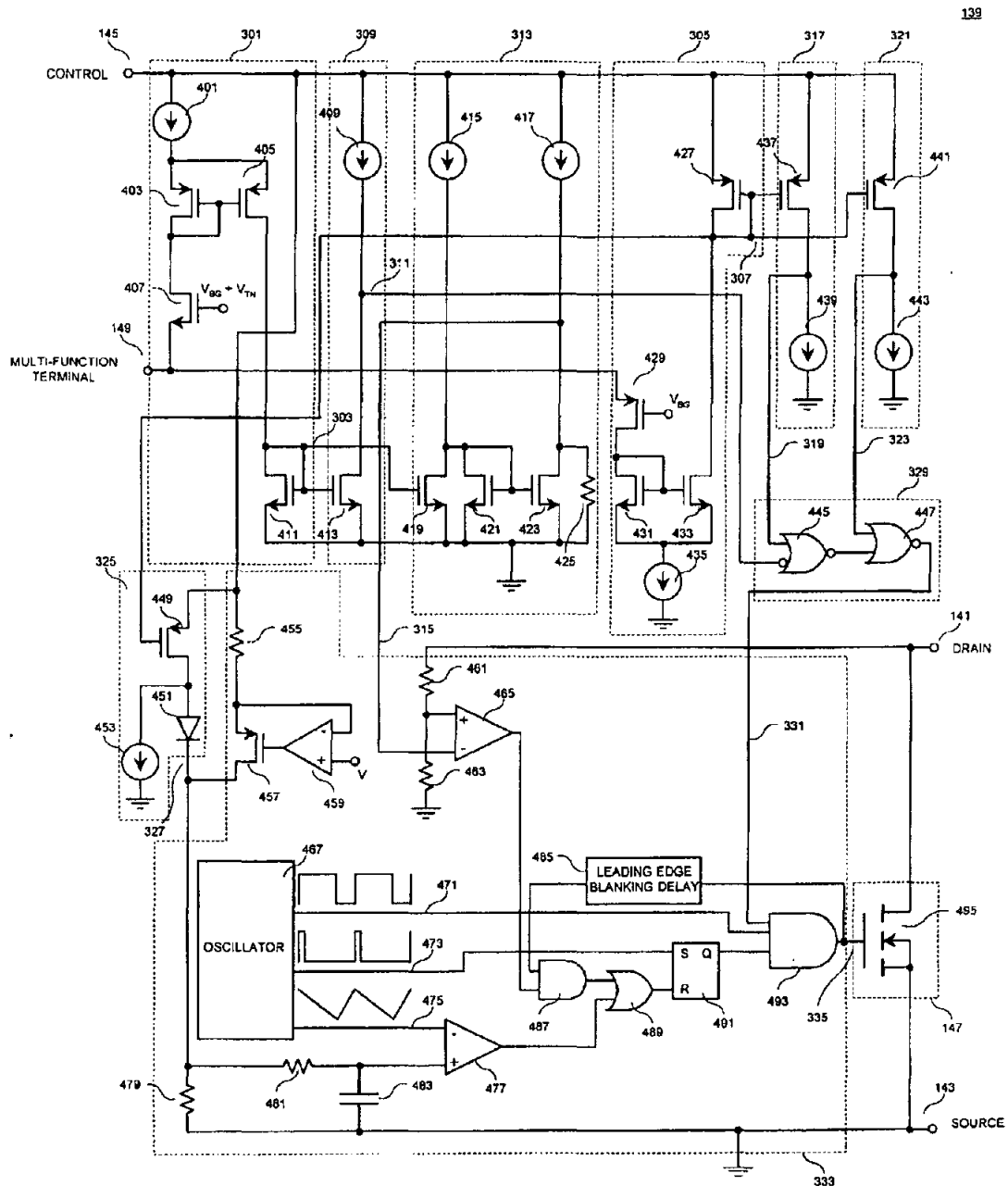


FIG. 7

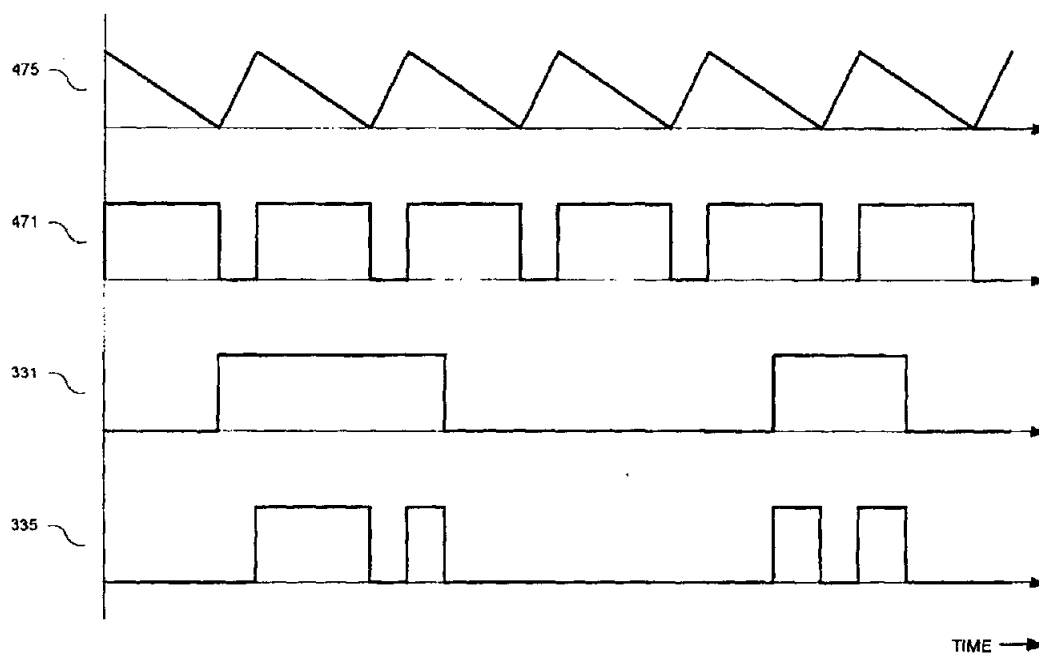


FIG. 8

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## METHOD AND APPARATUS PROVIDING A MULTI-FUNCTION TERMINAL FOR A POWER SUPPLY CONTROLLER

This is a Divisional of U.S. application Ser. No. 09/405, 209, filed Sep. 24, 1999, now pending.

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates generally to power supplies and, more specifically, the present invention relates to a switched mode power supply controller.

#### 2. Background Information

Electronic devices use power to operate. Switched mode power supplies are commonly used due to their high efficiency and good output regulation to power many of today's electronic devices. In a known switched mode power supply, a low frequency (e.g. 50 Hz or 60 Hz mains frequency), high voltage alternating current (AC) is converted to high voltage direct current (DC) with a diode rectifier and capacitor. The high voltage DC is then converted to high frequency (e.g. 30 to 300 kHz) AC, using a switched mode power supply control circuit. This high frequency, high voltage AC is applied to a transformer to transform the voltage, usually to a lower voltage, and to provide safety isolation. The output of the transformer is rectified to provide a regulated DC output, which may be used to power an electronic device. The switched mode power supply control circuit provides usually output regulation by sensing the output controlling it in a closed loop.

A switched mode power supply may include an integrated circuit power supply controller coupled in series with a primary winding of the transformer. Energy is transferred to a secondary winding from the primary winding in a manner controlled by the power supply controller to provide the clean and steady source of power at the DC output. The transformer of a switched mode power supply may also include another winding called a bias or feedback winding. The bias winding provides the operating power for the power supply controller and in some cases it also provides a feedback or control signal to the power supply controller. In some switched mode power supplies, the feedback or control signal can come through an opto-coupler from a sense circuit coupled to the DC output. The feedback or control signal may be used to modulate a duty cycle of a switching waveform generated by the power supply controller or may be used to disable some of the cycles of the switching waveform generated by the power supply controller to control the DC output voltage.

A power supply designer may desire to configure the power supply controller of a switched mode power supply in a variety of different ways, depending on for example the particular application and/or operating conditions. For instance, there may be one application in which the power supply designer would like the power supply controller to have one particular functionality and there may be another application in which the power supply designer would like the power supply controller to have another particular functionality. It would be convenient for power supply designer to be able to use the same integrated power supply controller for these different functions.

In order to provide the specific functions to the power supply controller, additional pins or electrical terminals are added for each function to the integrated circuit power supply controllers. Consequently, each additional function generally translates into an additional pin on the power

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supply controller chip, which translates into increased costs and additional external components. Another consequence of providing additional functionality to power supply controllers is that there is sometimes a substantial increase in power consumption by providing the additional functionality.

### SUMMARY OF THE INVENTION

Power supply controller methods and apparatuses are disclosed. In one embodiment, a power supply controller circuit is described including a current input circuit coupled to receive a current. In one embodiment, the current input circuit is to generate an enable/disable signal in response to the current. The power supply controller is to activate and deactivate the power supply in response to the enable/disable signal. In another embodiment, a current limit of a power switch of the power supply controller is adjusted in response to the current. In yet another embodiment, a maximum duty cycle of the power switch of the power supply is adjusted in response to the current. Additional features and benefits of the present invention will become apparent from the detailed description, figures and claims set forth below.

### BRIEF DESCRIPTION OF THE DRAWINGS

The present invention detailed illustrated by way of example and not limitation in the accompanying figures.

FIG. 1 is a schematic illustrating one embodiment of a power supply including a power supply controller having a multi-function terminal in accordance with the teachings of the present invention.

FIG. 2A is a schematic illustrating one embodiment of a power supply controller having a multi-function terminal configured to limit the current of the power switch in the power supply controller to a desired value in accordance with the teachings of the present invention.

FIG. 2B is a schematic illustrating one embodiment of a power supply having a multi-function terminal configured to provide a switchable on/off control to the power supply in accordance with the teachings of the present invention.

FIG. 2C is a schematic illustrating one embodiment of the power supply having a multi-function terminal configured to limit the current of the power switch in the power supply controller to a desired value and provide a switchable on/off control to the power supply controller in accordance with the teachings of the present invention.

FIG. 2D is a schematic illustrating one embodiment of a power supply having a multi-function terminal configured to provide line under-voltage detection, line over-voltage detection and maximum duty cycle reduction of the power supply in accordance with the teachings of the present invention.

FIG. 2E is a schematic illustrating one embodiment of a power supply having a multi-function terminal configured to provide line under-voltage detection, line over-voltage detection, maximum duty cycle reduction and a switchable on/off control to the power supply in accordance with the teachings of the present invention.

FIG. 2F is a schematic illustrating one embodiment of current mode control of a power supply controller having a multi-function terminal configured to regulate the current limit of the power switch in response to the power supply output in accordance with the teachings of the present invention.

FIG. 3 is a block diagram illustrating one embodiment of a power supply controller including a multi-function terminal in accordance with teachings of the present invention.

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FIG. 4 is a schematic illustrating one embodiment of a power supply controller including a multi-function terminal in accordance with the teachings of the present invention.

FIG. 5 is a diagram illustrating one embodiment of currents, voltages and duty cycles in relation to current through a multi-function terminal of a power supply controller in accordance with teachings of the present invention.

FIG. 6A is a diagram illustrating one embodiment of timing diagrams of switching waveforms of a power supply controller including a multi-function terminal in accordance with teachings of the present invention.

FIG. 6B is a diagram illustrating another embodiment of timing diagrams of switching waveforms of the power supply controller including a multi-function terminal in accordance with teachings of the present invention.

FIG. 7 is a schematic illustrating another embodiment of a power supply controller including a multi-function terminal in accordance with the teachings of the present invention.

FIG. 8 is a diagram illustrating another embodiment of timing diagrams of switching waveforms of the power supply controller including a multi-function terminal in accordance with teachings of the present invention.

#### DETAILED DESCRIPTION

A method and an apparatus providing a multi-function terminal in a power supply controller is disclosed. In the following description, numerous specifically details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific detail need not be employed to practice the present invention. In other instances, well-known materials or methods have not been described in detail in order to avoid obscuring the present invention.

In one embodiment of the present invention, a power supply controller is provided with the functionality of being able to remotely turn on and off the power supply. In another embodiment, the power supply controller is provided with the functionality of being able to externally set the current limit of a power switch in the power supply controller, which makes it easier to prevent saturation of the transformer reducing transformer size and cost. Externally settable current limit also allows the maximum power output to be kept constant over a wide input range reducing the cost of components that would otherwise have to handle the excessive power at high input voltages. In yet another embodiment, the power supply controller is provided with the functionality of being able to detect an under-voltage condition in the input line voltage of the power supply so that the power supply can be shutdown gracefully without any glitches on the output. In still another embodiment, the power supply controller is provided with the functionality of being able to detect an over-voltage condition in the input line voltage of the power supply so that the power supply can be shut down under this abnormal condition. This allows the power supply to handle much higher surge voltages due to the absence of reflected voltage and switching transients on the power switch in the power supply controller. In another embodiment, the power supply controller is provided with the functionality of being able to limit the maximum duty cycle of a switching waveform generated by a power supply controller to control the DC output of the power supply. In so doing, saturation of the transformer during power up is reduced and the excess power capability at high input voltages is safely limited. Increased duty cycle

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at low DC input voltages also allows for smaller input filter capacitance. Thus, this feature results in cost savings on many components in the power supply including the transformer. In yet another embodiment, some or all of the above functions are provided with a single multi-function terminal in the power supply controller. That is, in one embodiment, a plurality of additional functions are provided to power supply controller without the consequence of adding a corresponding plurality of additional terminals or pins to the integrated circuit package of the power supply controller. In one embodiment, one or some of the above functions are available when positive current flows into the multi-function terminal. In another embodiment, one or some of the above functions are available when negative current flows out from the multi-function terminal. In one embodiment, the voltage at the multi-function terminal is fixed at a particular value depending on whether positive current flows into the multi-function terminal or whether negative current flows out from the multi-function terminal.

The multi-function features listed above not only save cost of many components and improve power supply performance but also, they save many components that would otherwise be required if these features were implemented externally.

FIG. 1 is a block diagram illustrating one embodiment of a power supply 101 including a power supply controller 139 having a multi-function terminal 149 in accordance with the teachings of the present invention. As illustrated, power supply 101 includes an AC mains input 103, which is configured to receive an AC voltage input. A diode rectifier 105 is coupled to AC mains input to rectify the AC voltage. Capacitor 107 is coupled to diode rectifier 105 to convert the rectified AC into a steady DC line voltage 109, which is coupled to a primary winding 111 of a transformer. Zener diode 117 and diode 119 are coupled across primary winding 111 to provide clamp circuitry.

As illustrated in FIG. 1, primary winding 111 is coupled to a drain terminal 141 of power supply controller 139. Power supply controller 139 includes a power switch 147 coupled between the drain terminal 141 and a source terminal 143, which is coupled to ground. When power switch 147 is turned on, current flows through primary winding 111 of the transformer. When current flows through primary winding 111, energy is stored in the transformer. When power switch 147 is turned off, current does not flow through primary winding 111 and the energy stored in the transformer is transferred to secondary winding 113 and bias winding 115.

A DC output voltage is produced at DC output 125 through diode 121 and capacitor 123. Zener diode 127, resistor 129 and opto-coupler 131 form feedback circuitry or regulator circuitry to produce a feedback signal received at a control terminal 145 of the power supply controller 139. The feedback or control signal is used to regulate or control the voltage at DC output 125. As the voltage across DC output 125 rises above a threshold voltage determined by Zener diode 127, resistor 129 and opto-coupler 131, additional feedback current flows into control terminal 145. In one embodiment, control terminal 145 also provides a supply voltage for circuitry of power supply controller 139 through bias winding 115, diode 133, capacitor 135 and capacitor 137.

As shown in FIG. 1, power supply controller 139 includes a multi-function terminal 149, which in one embodiment enables power supply controller 139 to provide one or a plurality of different functions, depending on how multi-

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function terminal 149 is configured. Some examples of how multi-function terminal 149 may be configured are shown in FIGS. 2A through 2F.

For instance, FIG. 2A is a diagram illustrating one embodiment of a power supply controller 139 including a resistor 201 coupled between the multi-function terminal 149 and the source terminal 143. In one embodiment, the source terminal 143 is coupled to ground. In one embodiment, the voltage at multi-function terminal 149 is fixed when negative current flows from multi-function terminal 149. In one embodiment, the negative current that flows through resistor 201 is used to set externally the current limit of power switch 147. Thus, the power supply designer can choose a particular resistance for resistor 201 to set externally the current limit of power switch 147. In one embodiment, resistor 201 may be a variable resistor, a binary weighted chain of resistors or the like. In such embodiment, the current limit of power switch 147 may be adjusted externally by varying the resistance of resistor 201. In one embodiment, the current limit of power switch 147 is directly proportional to the negative current flowing through resistor 201.

FIG. 2B is a diagram illustrating another embodiment of a power supply controller 139 including a switch 203 coupled between multi-function terminal 149 and source terminal 143. In one embodiment, source terminal 143 is coupled to ground. In one embodiment, power supply controller 139 switches power switch 147 when multi-function terminal 149 is coupled to ground through switch 203. In one embodiment, power supply controller 139 does not switch power switch 147 when multi-function terminal 149 is disconnected from ground through switch 203. In particular, when an adequate amount of negative current flows from multi-function terminal 149, power supply 101 is enabled. When substantially no current flows from multi-function terminal 149, power supply 101 is disabled. In one embodiment, the amount of current that flows from multi-function terminal 149 to ground through switch 203 is limited. Thus, in one embodiment, even if multi-function terminal 149 is short-circuited to ground through switch 203, the amount of current flowing from multi-function terminal 149 to ground is limited to a safe amount.

FIG. 2C is a diagram illustrating yet another embodiment of a power supply controller 139 including resistor 201 and switch 203 coupled in series between multi-function terminal 149 and source terminal 143, which in one embodiment is ground. The configuration illustrated in FIG. 2C combines the functions illustrated and described in connection with FIGS. 2A and 2B above. That is, the configuration illustrated in FIG. 2C illustrates a power supply controller 139 having external adjustment of the current limit of power switch 147, through the selection of the resistance for resistor 201, and on/off functionality through switch 203. When switch 203 is on, power supply controller 139 will switch power switch 147 with a current limit set by resistor 201. When switch 203 is off, power supply controller 139 will not switch power switch 147 and power supply 101 will be disabled.

FIG. 2D is a diagram illustrating still another embodiment of a power supply controller 139 including a resistor 205 coupled between the line voltage 109 and multi-function terminal 149. Referring briefly back to FIG. 1 above, DC line voltage 109 is generated at capacitor 107 and is input to the primary winding 111 of the transformer of power supply 101. Referring back the FIG. 2D, in one embodiment, multi-function terminal 149 is substantially fixed at a particular voltage when positive current flows into multi-function terminal 149. Therefore, the amount of positive

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current flowing through resistor 205 into multi-function terminal 149 is representative of line voltage 109, which is input to the primary winding 111. Since the positive current flowing through resistor 205 into multi-function terminal 149 represents the line voltage 109, power supply controller 139 can use this positive current to sense an under-voltage condition in line voltage 109 in one embodiment. An under-voltage condition exists when the line voltage 109 is below a particular under-voltage threshold value. In one embodiment, if a line under-voltage condition is detected, power switch 147 is not switched by power supply controller 139 until the under-voltage condition is removed.

In one embodiment, power supply controller 139 can use the positive current flowing through resistor 205 into multi-function terminal 149 to detect an over-voltage condition in line voltage 109. An over-voltage condition when line voltage 109 rises above a particular over-voltage threshold value. In one embodiment, if a line over-voltage condition is detected, power switch 147 is not switched by power supply controller 139 until the over-voltage condition is removed.

In one embodiment, power supply controller 139 can also use the positive current flowing through resistor 205 and multi-function terminal 149 to detect for increases or decreases in line voltage 109. As line voltage 109 increases, for a given fixed maximum duty cycle, the maximum power available to secondary winding 113 in power supply 101 of FIG. 1 usually increases. As line voltage 109 decreases, less power is available to secondary winding 113 in power supply 101. In most cases, the excess power available at the DC output 125 is undesirable under overload conditions due to high currents that need to be handled by components. In some instances, it is also desirable to increase the maximum power available to DC output 125 at low input DC voltages to save on cost of the input filter capacitor 107. Higher duty cycle at low DC input voltage allows lower input voltage operation for a given output power. This allows larger ripple voltage on capacitor 107, which translates to a lower value capacitor. Therefore, in one embodiment, power supply controller 139 adjusts the maximum duty cycle of a switching waveform used to control or regulate power switch 147 in response to increases or decreases in line voltage 109. In one embodiment, the maximum duty cycle of the switching waveform used to control power switch 147 is inversely proportional to the line voltage 109. As mentioned earlier, reducing the duty cycle with increasing input DC voltage has many advantages. For instance, it reduces the value and hence the cost of capacitor 107. In addition, it limits excess power at high line voltages reducing the cost of the clamp circuit (117, 119), the transformer and the output rectifier 121 due to reduced maximum power ratings on these components.

It is appreciated that since only a single resistor 201 to ground, or a single resistor 205 to line voltage 109, is utilized for implementing some of the functions of power supply controller 139, a power savings is realized. For instance, if a resistor divider were to be coupled between power and ground, and a voltage output of the resistor divider coupled to a terminal of power supply controller 139 were to be used, current would continuously flow through both the resistor divider and into a sensor terminal of the power supply controller. This would result in increased power consumption. However in one embodiment of the power supply controller 139, only the single resistor 201 to ground or single resistor 205 to line voltage 109 is utilized, thereby eliminating the need for a current to flow through both the resistor divider and into power supply controller 139.

1 Plaintiff Power Integrations, Inc. hereby alleges as follows:

2 **THE PARTIES**

3 1. Power Integrations, Inc. ("Power Integrations") is incorporated under the laws of the  
4 state of Delaware, and has a regular and established place of business at 5245 Hellyer Avenue, San  
5 Jose, California 95138.

6 2. Upon information and belief, defendant Fairchild Semiconductor International, Inc.  
7 is incorporated under the laws of the state of Delaware, with its headquarters located at 82 Running  
8 Hill Road, South Portland, Maine, 04106.

9 3. Upon information and belief, defendant Fairchild Semiconductor Corporation is  
10 incorporated under the laws of the state of Delaware, with its headquarters located at 82 Running  
11 Hill Road, South Portland, Maine, 04106.

12 4. Upon information and belief, defendant System General Corporation (hereinafter  
13 "SG") is incorporated under the laws of Taiwan, with its headquarters located at 5F, No. 9, Alley 6,  
14 Lane 45 Bao Shing Road, Shin Dian, Taipei, Taiwan. Upon information and belief, SG is a wholly  
15 owned subsidiary of Fairchild Semiconductor Corporation.

16 5. Defendant Fairchild Semiconductor International, Inc., defendant Fairchild  
17 Semiconductor Corporation, and defendant SG will hereinafter be collectively referred to as  
18 "Defendants."

19 **JURISDICTION AND VENUE**

20 6. This action arises under the patent laws of the United States, Title 35 U.S.C. § 1 *et*  
21 *seq.* This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

22 7. Upon information and belief, this Court has personal jurisdiction over Defendants  
23 because Defendants have purposely availed themselves of the privilege of conducting activities  
24 within this State and judicial District.

25 8. Upon information and belief, venue is proper in this Court pursuant to 28 U.S.C.  
26 §§ 1391(b), 1391(c) and 1400 because the Defendants are subject to personal jurisdiction in this  
27 judicial District.

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FIG. 2E is a diagram illustrating yet another embodiment of a power supply controller 139 including resistor 205, as described above, coupled between the line voltage 109 and multi-function terminal 149. FIG. 2E also includes a switch 207 coupled between control terminal 145 and multi-function terminal 149. In one embodiment, resistor 205 provides the same functionality as discussed above in connection with FIG. 2D. Therefore, when switch 207 is switched off, the configuration illustrated in FIG. 2E is identical to the configuration described above in connection with FIG. 2D.

In one embodiment, control terminal 145 provides a supply voltage for power supply controller 139 in addition to providing a feedback or control signal to power supply controller 139 from DC output 125. As a result, in one embodiment, switch 207 provides in effect a switchable low resistance connection between a supply voltage (control terminal 145) and multi-function terminal 149. In one embodiment, the maximum positive current that can flow into multi-function terminal 149 is limited. Therefore, in one embodiment, even when switch 207 provides, in effect, a short-circuit connection from a supply voltage, the positive current that flows into multi-function terminal 149 is limited to a safe amount. However, in one embodiment, the positive current that does flow through switch 207, when activated, into multi-function terminal 149 triggers an over-voltage condition. As discussed above, power supply 139 discontinues switching power switch 147 during an over-voltage condition until the condition is removed. Therefore, switch 207 provides on/off functionality for power supply controller 139. When switch 207 is the activated, the low resistance path to control terminal 145 is removed and the positive current flowing into multi-function terminal 149 is limited to the current that flows from line voltage 109 through resistor 205. Assuming that neither an under-voltage condition nor an over-voltage condition exists, power supply controller 139 will resume switching power switch 147, thereby re-enabling power supply 101.

FIG. 2F is a diagram illustrating another embodiment of a power supply controller 139 using current mode control to regulate the current limit of the power supply. As shown, resistor 201 is coupled between the multi-function terminal 149 and the source terminal 143 and the transistor 209 of an opto-coupler coupled between multi-function terminal 149 and a bias supply, such as for example control terminal 145. Similar to FIG. 2A, the negative current that flows out from multi-function terminal 149 is used to set externally the current limit of power switch 147. In the embodiment illustrated in Figure in FIG. 2F, the current limit adjustment function can be used for controlling the power supply output by feeding a feedback signal from the output of the power supply into multi-function terminal 149. In the embodiment depicted in FIG. 2F, the current limit is adjusted in a closed loop to regulate the output of the power supply (known as current mode control) by adding the opto-coupler output between multi-function terminal 149 and the bias supply.

In one embodiment, the power supply controller configurations described in connection with FIGS. 2A through 2F all utilize the same multi-function terminal 149. Stated differently, in one embodiment, the same power supply controller 139 may be utilized in all of the configurations described. Thus, the presently described power controller 139 provides a power supply designer with added flexibility. As a result, a power supply designer may implement more than one of the above functions at the same time using the presently described power supply controller 139. In addition, the same functionality may be implemented in

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more than one way. For example, power supply 101 can be remotely turned on and off using either power or ground. In particular, the power supply 101 can be turned on and off by switching to and from the control terminal (supply terminal for the power supply controller) using the over-voltage detection feature, or by switching to and from ground using the on/off circuitry.

FIGS. 2A through 2F provide just a few examples of use of the multi-function terminal. A person skilled in the art will find many other configurations for use of the multi-function pin. The uses for the multi-function terminal, are therefore, not limited to the few examples shown.

It is worthwhile to note that different functions of the presently described power supply controller 139 may be utilized at different times during different modes of operation of power supply controller 139. For instance, some features may be implemented during startup operation, other functions may be implemented during normal operation, while still other functions may be implemented during standby operation. Indeed, it is appreciated that a power supply designer may implement other circuit configurations to use with a power supply controller 139 in accordance with teachings of the present invention. The configurations illustrated in FIGS. 2A through 2F are provided simply for explanation purposes.

FIG. 3 is a block diagram illustrating one embodiment of a power supply controller 139 in accordance with teachings of the present invention. As shown in the embodiment illustrated, power supply controller 139 includes a current input circuit 302, which in one embodiment serves as multi-function circuitry. In one embodiment, current input circuit 302 includes a negative current input circuit 304 and a positive current input circuit 306. In one embodiment, negative current input circuit 304 includes negative current sensor 301, on/off circuitry 309 and external current limit adjuster 313. In one embodiment, positive current input circuit 306 includes positive current sensor 305, under-voltage comparator 317, over-voltage comparator 321 and maximum duty cycle adjuster 325.

As shown in FIG. 3, negative current sensor 301 and positive current sensor 305 are coupled to multi-function terminal 149. In one embodiment, negative current sensor 301 generates a negative current sense signal 303 and positive current sensor generates a positive current sense signal 307. For purposes of this description, a negative current may be interpreted as current that flows out of multi-function terminal 149. Positive current may be interpreted as current that flows into multi-function terminal 149. In one embodiment, on/off circuitry 309 is coupled to receive negative current sense signal 303. External current limit adjuster 313 is coupled to receive negative current sense signal 303.

In one embodiment, under-voltage comparator 317 is coupled to receive positive current sense signal 307. Over-voltage comparator 321 is coupled to receive positive current sense signal 307. As discussed earlier, both under-voltage and over-voltage comparators also function as on/off circuits. Maximum duty cycle adjuster 325 is also coupled to receive positive current sense signal 307.

In one embodiment, on/off circuitry 309 generates an on/off signal 311, under-voltage comparator 317 generates an under-voltage signal 319 and over-voltage comparator 321 generates an over-voltage signal 323. As shown in the embodiment illustrated in FIG. 3, enable/disable logic 329 is coupled to receive the on/off signal 311, the under-voltage



signal 319 and the over-voltage signal 323. The under-voltage and over-voltage signals can also be used for on/off functions as noted earlier.

In one embodiment, enable/disable logic 329 generates an enable/disable signal 331, which is coupled to be received by control circuit 333. The control circuit 333 is also coupled to receive a control signal from control terminal 145. In addition, control circuit 333 is also coupled to receive a drain signal from drain terminal 141, a maximum duty cycle adjustment signal 327 from maximum duty cycle adjuster 325 and an external current limit adjustment signal 315 from external current limit adjuster 313.

In one embodiment, control circuit 333 generates a switching waveforms 335, which is coupled to be received by power switch 147. In one embodiment, power switch 147 is coupled between drain terminal 141 and source terminal 143 to control a current flowing through the primary winding 111 of power supply 101, which is coupled to drain terminal 141.

In one embodiment, negative current sensor 301 senses current that flows out of negative current sensor 301 through multi-function terminal 149. Negative current sense signal 303 is generated in response to the current that flows from negative current sensor 301 through multi-function terminal 149. In one embodiment, current that flows from negative current sensor 301 through multi-function terminal 149 typically flows through an external resistance or switch coupled between multi-function terminal 149 and ground.

In one embodiment, positive current sensor 305 senses current that flows into positive current sensor 305 through multi-function terminal 149. Positive current sense signal 307 is generated in response to the current that flows into positive current sensor 305 through multi-function terminal 149. In one embodiment, current that flows into positive current sensor 305 through multi-function terminal 149 typically flows through an external resistance coupled between multi-function terminal 149 and the DC line voltage 109 input to the primary winding 111 of a power supply 101 and/or another voltage source. In another embodiment the current flows through an external resistance or a switch coupled between the multi-function terminal 149 and another voltage source. In one embodiment, the line voltage 109 input to primary winding 111 is typically a rectified and filtered AC mains signal.

As mentioned above, in one embodiment, positive current does not flow while negative current flows, and vice versa. In one embodiment, the negative current sensor 301 and positive current sensor 305 are designed in such a way that they are not active at the same time. Stated differently, negative current sense signal 303 is not active at the same time as positive current sense signal 307 in one embodiment.

In one embodiment, the voltage at multi-function terminal 149 is fixed at a first level when negative current flows out of power supply controller 139 from multi-function terminal 149. In one embodiment, the first level is selected to be approximately 1.25 volts. In one embodiment, the voltage at multi-function terminal is fixed at a second level when positive current flows into power supply controller 139 through multi-function terminal 149. In one embodiment, the second level is selected to be approximately 2.3 volts.

In one embodiment, on/off circuitry 309 generates on/off signal 311 in response to negative current sense signal 303. In one embodiment, when the current flowing from multi-function terminal 149 through an external resistance to ground is less than a predetermined on/off threshold level, on/off circuitry 309 generates on/off signal 311 to switch off

the power supply 101. In one embodiment, when the current flowing from multi-function terminal 149 is greater than a predetermined on/off threshold level, on/off circuitry 309 generates on/off signal 311 to switch on the power supply 101. In one embodiment, the magnitude of the on/off threshold level is approximately 40 to 50 microamps, including hysteresis.

In one embodiment, external current limit adjuster 313 generates external current limit adjustment signal 315 in response to negative current sense signal 303. In one embodiment, when the magnitude of the negative current flowing from multi-function terminal 149 through an external resistance or switch to ground is below a predetermined level, the current limit adjuster 313 generates an external current limit adjustment signal to limit the current flowing through power switch 147. In one embodiment, when the magnitude of the negative current flowing from multi-function terminal 149 is below a predetermined level, the current flowing through power switch 147 is limited to an amount directly proportional to the current flowing out of power supply controller 139 from multi-function terminal 149. In one embodiment, predetermined level is approximately 150 microamps. In one embodiment, if the magnitude of the negative current flowing out of power supply controller 139 from multi-function terminal 149 is greater than the predetermined level, the current flowing through power switch 147 is internally limited or clamped to a fixed safe maximum level. Therefore, the current flowing through power switch 147 is clamped to a safe value, even when multi-function terminal 149 is shorted to ground. In one embodiment, the current flowing through power switch 147 is internally limited or clamped to value of 3 amps.

In one embodiment, since the voltage at multi-function terminal 149 is fixed at a particular voltage when current flows out of power supply controller 139 through multi-function terminal 149, the current limit through power switch 147 can be accurately set externally with a single large value, low-cost, resistor externally coupled between multi-function terminal 149 and ground. By using a large external resistance, the current flowing from multi-function terminal 149 is relatively small. As mentioned above, the current flowing from multi-function terminal 149 in one embodiment is in the microamp range. Since the current flowing from multi-function terminal 149 is relatively small, the amount of power dissipated is also relatively small.

In one embodiment, multi-function terminal 149 is coupled to the DC line voltage 109 input to the primary winding 111 through an external resistance. In one embodiment, the amount of current flowing into multi-function terminal 149 represents the DC input line voltage to the power supply 101. In one embodiment, under-voltage comparator 317 generates under-voltage signal 319 in response to the resulting positive current sense signal 307. In one embodiment, when the current flowing into multi-function terminal 149 rises above a first predetermined threshold, under-voltage comparator 317 generates under-voltage signal 319 to enable the power supply. In one embodiment, when the current flowing into multi-function terminal 149 falls below a second predetermined threshold, under-voltage comparator 317 generates under-voltage signal 319 to disable the power supply. In one embodiment, the first predetermined threshold is greater than the second predetermined threshold to provide hysteresis. By providing hysteresis or a hysteretic threshold, unwanted switching on and off of the power supply 101 resulting from noise or ripple is reduced. In one embodiment, the first predetermined threshold is approximately 50 microamps and the

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second predetermined threshold is approximately 0 microamps. In another embodiment, a hysteretic threshold is not utilized. Thus the hysteresis is greater than or equal to zero.

In one embodiment, over-voltage comparator 321 generates overvoltage signal 323 in response to the positive current sense signal 307. In one embodiment, when the current flowing into multi-function terminal 149 rises above a third predetermined threshold, over-voltage comparator 321 generates over-voltage signal 323 to disable the power supply. In one embodiment, when the current flowing into multi-function terminal 149 falls below a fourth predetermined threshold, over-voltage comparator 321 generates over-voltage signal 323 to enable the power supply. In one embodiment, the third predetermined threshold is greater than the fourth predetermined threshold to provide hysteresis. By providing hysteresis or a hysteretic threshold, unwanted switching on and off of the power supply resulting from noise is reduced. In one embodiment, the third predetermined threshold is approximately 225 microamps and the fourth predetermined threshold is approximately 215 microamps. In one embodiment, the third and fourth predetermined thresholds are selected to be approximately four to five times greater than the first predetermined threshold discussed above for an AC mains input 103 of approximately 85 volts to 265 volts AC. In another embodiment, a hysteretic threshold is not utilized. Thus the hysteresis is greater than or equal to zero.

In one embodiment, power switch 147 is able to tolerate higher voltages when not switching. When the power supply is disabled, power switch 147 does not switch. Therefore, it is appreciated that over-voltage comparator 321 helps to protect the power supply 101 from unwanted input power surges by disabling the power switch 147.

In one embodiment, over-voltage and under-voltage comparators 321 and 317 may also be used for on/off functionality, similar to on/off circuitry 309. In particular, multi-function terminal 149 may be switchably coupled to a on/off control signal source to provide a positive current that flows into multi-function terminal 149 that cross the under-voltage or over-voltage thresholds (going above the third or below the fourth predetermined thresholds). For example, when the positive current through the multi-function pin crosses above the first predetermined threshold of the under-voltage comparator 317, the power supply will be enabled and when the positive current goes below the second predetermined threshold of the under-voltage comparator 317, the power supply is disabled. Similarly, when the positive current through the multi-function pin crosses above the third predetermined threshold of the over-voltage comparator 321, the power supply will be disabled and when the positive current goes below the fourth predetermined threshold of the over-voltage comparator 321, the power supply is enabled.

In one embodiment, maximum duty cycle adjuster 325 generates maximum duty cycle adjustment signal 327 in response to the positive current sense signal 307. In one embodiment, maximum duty cycle adjustment signal 327, which is received by control circuit 333, is used to adjust the maximum duty cycle of the switching waveform 335 used to control power switch 147. In one embodiment, the maximum duty cycle determines how long a power switch 147 can be on during each cycle. For example, if the maximum duty cycle is 50 percent, the power switch 147 can be on for a maximum of 50 percent of each cycle.

Referring briefly for example to the power supply 101 of FIG. 1, while power switch 147 is on, power is stored in the

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transformer core through the primary winding 111. While the power switch 147 is off, power is delivered from the transformer core to the secondary winding of the transformer in power supply 101. To delivery a given power level, for a lower DC input voltage 109, a higher duty cycle is required and for a higher DC input voltage 109, a lower duty cycle is required. In one embodiment of the present invention, maximum duty cycle adjuster 325 decreases the maximum duty cycle of power switch 147 in response to increases in the DC input voltage 109. In one embodiment, maximum duty cycle adjuster 325 increases the maximum duty cycle of power switch 147 in response to decreases in the DC input voltage 109. Stated differently, the maximum duty cycle is adjusted to be inversely proportional to the current that flows into multi-function terminal 149 in one embodiment of the present invention.

Referring back to FIG. 3, in one embodiment, the maximum duty cycle is adjusted within a range of 33 percent to 75 percent based on the amount of positive current that flows into multi-function terminal 149. In one embodiment, maximum duty cycle adjuster 325 does not begin to decrease the maximum duty cycle until the amount of current that flows into multi-function terminal 149 rises above a threshold value. In one embodiment, that threshold value is approximately 60 microamps. In one embodiment, the maximum duty cycle is not adjusted if negative current flows out of multi-function terminal 149. In this case, the maximum duty cycle is fixed at 75 percent in one embodiment of the present invention.

In one embodiment, enable/disable logic 329 receives as input on/off signal 311, under-voltage signal 319 and over-voltage signal 323. In one embodiment, if any one of the under-voltage or over-voltage conditions exist, enable/disable logic 329 disables power supply 101. In one embodiment, when the under-voltage and over-voltage conditions are removed, enable/disable logic 329 enables power supply 101. In one embodiment, power supply 101 may be enabled or disabled by starting and stopping, respectively, the switching waveform 335 at the beginning of a switching cycle just before the power switch is to be turned on. In one embodiment, enable/disable logic 329 generates enable/disable signal 331, which is received by the oscillator in the control circuit 333 to start or stop the oscillator at the beginning of a switching cycle of switching waveform 335. When enabled the oscillator will start a new on cycle of the switching waveform. When disabled the oscillator will complete the current switching cycle and stop just before the beginning of the next cycle.

In one embodiment, control circuit 333 generates switching waveform 335 to control power switch 147 in response to a current sense signal received from drain terminal 141, enable/disable signal 331, maximum duty cycle adjustment signal 327, a control signal from control terminal 145 and external current limit adjustment signal 315.

In one embodiment, the enable/disable signal can also be used to synchronize the oscillator in the control circuit to an external on/off control signal source having a frequency less than that of the oscillator. The on/off control signal can be input to the multi-function terminal through any of the three paths that generate the enable/disable signal: on/off circuitry 309, under-voltage comparator 317 or over-voltage comparator 321. As discussed, enable/disable the oscillator in the control circuit 333, in one embodiment, begins a new complete cycle of switching waveform at 335 using known techniques in response to enable/disable signal 331, which represents the on/off control signal at the multi-function input. By turning the on/off control signal "on" at the

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multi-function input for a fraction of the switching cycle and then "off," the oscillator is enabled to start a new complete cycle. Therefore, if the external on/off control signal has short "on" pulses at a frequency less than the oscillator in the control circuit, the oscillator will produce a switching cycle each time an on pulse is detected, thus providing a switching waveform that is synchronized to the external frequency.

In an alternate embodiment shown below in FIG. 7, the enable/disable signal 331 directly disables or turns off the power switch through the AND gate 493 when an under-voltage or over-voltage condition exists. In this embodiment, the power switch can be enabled or disabled in the middle of a cycle and consequently, synchronization of the switching waveform through a on/off control signal at the multi-function input is not provided.

FIG. 4 is a schematic of one embodiment of a power supply controller 139 in accordance with the teachings of the present invention. As illustrated, negative current sensor 301 includes a current source 401 coupled to control terminal 145. Transistors 403 and 405 form a current mirror coupled to current source 401. In particular, transistor 403 has a source coupled to current source 401 and a gate and drain coupled to the gate of transistor 405. The source of transistor 405 is also coupled to current source 401. Transistor 407 is coupled between the drain and gate of transistor 403 and multi-function terminal 149. In one embodiment, the gate of transistor 407 is coupled to a band gap voltage  $V_{BG}$ . Plus a threshold voltage  $V_{TN}$ . In one embodiment,  $V_{BG}$  is approximately 1.25 volts,  $V_{TN}$  is approximately 1.05 volts and  $V_{BG}+V_{TN}$  is approximately 2.3 volts. Transistors 411 and 413 also form a current mirror coupled to the drain of transistor 405. In particular, the gate and drain of transistor 411 are coupled to the drain of transistor 405 and the gate of transistor 413. In one embodiment, negative current sense signal 303 is generated at the gate and drain of transistor 411. The sources of transistors 411 and 413 are coupled to ground. In one embodiment, ground is provided through source terminal 143.

In one embodiment, on/off circuitry 309 includes a current source 409 coupled between the drain of transistor 413 and control terminal 145. In one embodiment, on/off signal 311 is generated at the drain of transistor 413.

In one embodiment, external current limit adjuster 313 includes a current source 415 coupled between control terminal 145 and the drain of transistor 419 and the gate and drain of transistor 421. The source of transistor 419 and the source of transistor 421 are coupled to ground. The gate of transistor 419 is coupled to receive negative current sense signal 303. External current limit adjuster 313 also includes a current source 417 coupled between control terminal 145 and the drain of transistor 423 and resistor 425. The source of transistor 423 and resistor 425 are coupled to ground. External current limit adjustment signal 315 is generated at the drain of transistor 423.

In one embodiment, positive current sensor 305 includes transistor 429 having a source coupled to multi-function terminal 149 and the current mirror formed with transistors 431 and 433. In particular, transistor 431 has a gate and drain coupled to the drain of transistor 429 and the gate of transistor 433. Current source 435 is coupled between ground and the sources of transistors 431 and 433. The gate of transistor 429 is coupled to band gap voltage  $V_{BG}$ . The drain of transistor 433 is coupled to the current mirror formed with transistors 427 and 437. In particular, the gate and drain of transistor 427 are coupled to the gate of transistor 437 and the drain of transistor 433. The sources of

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transistors 427 and 437 are coupled to control terminal 145. Positive current sense signal 307 is generated at the gate and drain of transistor 427.

In one embodiment, under-voltage comparator 317 includes a current source 439 coupled between the drain of transistor 437 and ground. Under-voltage signal 319 is generated at the drain of transistor 437.

In one embodiment, over-voltage comparator 321 includes a current source 443 coupled between the drain of transistor 441 and ground. Transistor 441 has a source coupled to control terminal 145 and a gate coupled to receive positive current sense signal 307. Over-voltage signal 323 is generated at the drain of transistor 441.

In one embodiment, enable/disable logic 329 includes NOR gate 445 having an input coupled to receive under-voltage signal 319 and an inverted input coupled to receive on/off signal 311. Enable/disable logic 329 also includes NOR gate 447 having an input coupled to receive over-voltage signal 323 and an input coupled to an output of NOR gate 445. Enable/disable signal 331 is generated at the output of NOR gate 447.

In one embodiment, maximum duty cycle adjuster 325 includes a transistor 449 having a source coupled to control terminal 145 and a gate coupled to receive positive current sense signal 307. Maximum duty cycle adjuster 325 also includes a current source 453 coupled between the drain of transistor 449 and ground. A diode 451 is coupled to the drain of transistor 449 to produce maximum duty cycle adjustment signal 327.

In one embodiment, power switch 147 includes a power metal oxide semiconductor field effect transistor (MOSFET) 495 coupled between drain terminal 141 and source terminal 143. Power MOSFET 495 has a gate coupled to receive a switching waveform 335 generated by pulse width modulator 333.

In one embodiment, control circuit 333 includes a resistor 455 coupled to the control terminal 145. A transistor 457 has a source coupled to resistor 455 and a negative input of a comparator 459. A positive input of comparator 459 is coupled to a voltage  $V$ , which in one embodiment is approximately 5.7 volts. An output of comparator 459 is coupled to the gate of transistor 457. The drain of transistor 457 is coupled to diode 451 and resistor 479. The other end resistor 479 is coupled to ground. A filter is coupled across resistor 479. The filter includes a resistor 481 coupled to resistor 479 and capacitor 483 coupled to resistor 481 and ground. Capacitor 483 is coupled to a positive input of comparator 477.

In one embodiment, control circuit 333 is a pulse width modulator, which has an oscillator 467 with three oscillating waveform outputs 471, 473 and 475. Oscillator 467 also includes an enable/disable input 469 coupled to receive enable/disable signal 331. In one embodiment, control circuit 333 also includes a voltage divider including resistors 461 and 463 coupled between drain terminal 141 and ground. A node between resistors 461 and 463 is coupled to a positive input of a comparator 465. A negative input of comparator 465 is coupled to receive external current limit adjustment signal 315.

In one embodiment, oscillating waveform output 471 is coupled to a first input of AND gate 493. Oscillating waveform output 473 is coupled to a set input of latch 491. Oscillating waveform output 475 is coupled to a negative input of comparator 477. An output of comparator 465 is coupled to a first input of AND gate 487. A leading edge blanking delay circuit 485 is coupled between the output of

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NAND gate 493 and a second input of AND gate 487. In one embodiment, there is a gate driver or a buffer between the output of the NAND gate 493 and the gate of the MOSFET (not shown). An output of AND gate 487 is coupled to a first input of OR gate 489. A second input of OR gate 489 is coupled to an output of comparator 477. An output of OR gate 489 is coupled to a reset input of latch 491. An output of latch 491 is coupled to a second input of AND gate 493. The output of AND gate 493 generates switching waveform 335.

Operation of power supply controller 139 of FIG. 4 is as follows. Beginning with negative current sensor 301, the gate of transistor 407 is fixed at  $V_{BG} + V_{TN}$  in one embodiment to approximately 2.3 volts. As a result, transistor 407 sets the voltage at multi-function terminal 149 to  $V_{BG}$  in one embodiment, which is approximately 1.25 volts, when current is pulled out of multi-function terminal 149. This current may be referred to as negative current since the current is being pulled out of power supply controller 139. In one embodiment, transistor 407 is sized such that it operates with a current density resulting in a voltage drop between the gate and source that is close to  $V_{TN}$ , wherein the  $V_{TN}$  is the threshold of the N channel transistor 407, when negative current flows from multi-function terminal 149. When an external resistor (not shown) is coupled from multi-function terminal 149 to ground, the negative current flowing through the external resistor will therefore be  $V_{BG}$  divided by the value of the external resistor in accordance with Ohm's law. This negative current flowing out from multi-function terminal 149 passes through transistors 403 and is mirrored on to transistor 405. Current source 401 limits the negative current sourced by multi-function terminal 149. Therefore, even if multi-function terminal 149 is short-circuited to ground, the current is limited to a current less than the current supplied by current source 401. This current is less than the current source 401 by an amount that flows through the transistor 405. In one embodiment, the negative current that can be drawn from the multi-function terminal is limited to 200 microamps by the current source 401. In one embodiment, if more negative current than current source 401 is able to supply is pulled from multi-function terminal 149, the voltage at multi-function terminal 149 collapses to approximately 0 volts.

The current that flows through transistor 403 is mirrored to transistor 405. The current that flows through transistors 405 and 411 is the same since they are coupled in series. Since transistors 411 and 413 form a current mirror, the current flowing through transistor 413 is proportional to the negative current flowing through multi-function terminal 149. The current flowing through transistor 413 is compared to the current provided by current source 409. If the current through transistor 413 is greater than the current supplied by current source 409, the signal at the drain of transistor 413 will go low, which in one embodiment enables the power supply. Indeed, on/off signal 311 is received at an inverted input of NOR gate 445. Thus, when on/off signal 311 is low, the power supply is enabled. Therefore, by having a negative current greater than a particular threshold value, the power supply of the present invention is enabled in one embodiment. In one embodiment, the magnitude of that particular threshold value is approximately 50 microamps.

As mentioned above, the current flowing through transistor 411 is proportional to the negative current flowing out from multi-function terminal 149. As illustrated, transistor 419 also forms a current mirror with transistor 411. Therefore, the current flowing through transistor 419 is proportional to the current flowing through transistor 411.

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The current flowing through transistor 421 is the difference between the current supplied by current source 415 and the current flowing through transistor 419. For example, assume that the current supplied by current source 415 is equal to A. Assume further that the current flowing through transistor 419 is equal to B. In this case, the current flowing through transistor 421 is equal to A-B.

As illustrated, transistor 423 forms a current mirror with transistor 421. Therefore, the current flowing through transistor 423 is proportional to the current flowing through transistor 421. Continuing with the example above and assuming further that transistors 421 and 423 are equal in size, the current flowing through transistor 423 is also equal to A-B. Assuming further that current source 417 supplies a current equal to the current supplied by current source 415, which is assumed to be equal to A, then the current flowing through resistor 425 would be equal to A-(A-B), which is equal to B.

Therefore, the current flowing through resistor 425 is proportional to the current flowing through transistor 419, which is proportional to the current flowing through transistor 411, which is proportional to the negative current flowing out from multi-function terminal 149. Note that if the current flowing through transistor 419 is greater than the current supplied by current source 415, the current flowing through transistor 421 would be zero because the voltage at the drains of transistors 419 and 421 would collapse to approximately zero volts. This would result in the current flowing through transistor 423 to be zero. Thus, the current through resistor 425 cannot be greater than the current supplied by current source 417. However, as long as B is less than A, the current that flows through resistor 425 is equal to B. If B rises above A, the current that flows through resistor 425 is equal to A.

In one embodiment, resistor 425 is fabricated using the same or similar types of processes and diffusions or doped regions used in fabricating power MOSFET 495. As a result, the on resistance of resistor 425 follows or tracks the on resistance of power MOSFET 495 through varying operating conditions and processing variations.

The voltage across resistor 425 is reflected in external current limit adjuster signal 315, which is input to the negative input of comparator 465. In one embodiment, the negative input of comparator 465 is the threshold input of comparator 465. Therefore, the negative input of comparator 465 receives a voltage proportional to the negative current flowing out of multi-function terminal 149 multiplied by the resistance of resistor 425.

The positive input of comparator 465 is coupled to drain terminal 141 through resistor 461 of the voltage divider formed by resistor 461 and resistor 463. Therefore, the positive input of comparator 465 senses a voltage proportional to the drain current of power MOSFET 495 multiplied by the on resistance of power MOSFET 495.

When the voltage at the positive terminal of comparator 465 rises above the voltage provided by external current limit adjuster signal 315 to the negative terminal of comparator 465, the output of comparator 465 is configured to reset latch 491 through AND gate 487 and OR gate 489. By resetting latch 491, the on portion of a cycle of waveform 335 received at the gate of power MOSFET 495 is masked or cut short, which results in turning off power MOSFET 495 when the amount of current flowing through power switch 147 rises above the threshold.

In one embodiment, AND gate 487 also receives input from leading edge blanking delay circuitry 485. In one

embodiment, leading edge blanking delay circuitry 485, using known techniques, temporarily disables current limit detection at the start, or during the leading edge portion, of an on transition of power MOSFET 495.

As shown in the embodiment illustrated in FIG. 4, latch 491 is set at the beginning of each cycle by switching waveform output 473. One way that latch 491 is reset, thereby turning off power MOSFET 495, is through the output of comparator 465. Another way to reset latch 491 is through the output of comparator 477, which will be discussed below in connection with maximum duty cycle adjuster 325.

With regard to positive current sensor 305, the gate of transistor 429 is coupled to the band gap voltage  $V_{BG}$ . In one embodiment, transistor 429 is sized such that it operates with a current density resulting in a drop between the source and gate close to  $V_{TP}$ , which is threshold of the P channel transistor 429, when positive current flows into multi-function terminal 149. In one embodiment, current that flows into multi-function terminal 149 is referred to as positive current since the current is being fed into the power supply controller 139. As a result, the voltage at multi-function terminal 149 is fixed at approximately  $V_{BG} + V_{TP}$  when positive current flows into multi-function terminal 149.

The gate voltages on the transistors 407 and 429 chosen in the embodiment discussed above are such that only one of transistors 407 and 429 are switched on at a time depending on the polarity of the current at the multi-function terminal. Stated differently, if transistor 407 is on, transistor 429 is off. If transistor 429 is on, transistor 407 is off. As result, if negative current sensor 301 is on, positive current sensor 305 is isolated from multi-function terminal 149. If positive current sensor 305 is on, negative current sensor 301 is isolated from multi-function terminal 149. Therefore, if there is negative current flowing through multi-function terminal 149, positive current sensor 305 is disabled. If there is positive current flowing through multi-function terminal 149, negative current sensor 301 is disabled.

In one embodiment, the positive current that flows into transistor 429 flows through transistor 431 since they are coupled in series. The positive current through multi-function terminal 149 flows into and is limited by current source 435. In one embodiment, if the positive current through multi-function terminal 149 is greater than an amount that current source 435 can sink minus the current in transistor 433, then the voltage at multi-function terminal 149 will rise and is clamped either by the circuitry driving the current or by the standard clamping circuitry that is used for protection purposes on external terminals such as the multi-function terminal, of a power supply controller. As shown, transistors 431 and 433 form a current mirror. Therefore, the current flowing through transistor 433 is proportional to the positive current that flows through transistor 431. The current that flows through the transistor 433 flows to transistor 427 since they are coupled in series. As shown, the gate of transistor 427 is coupled to the drain of transistor 427, which generates positive current sense signal 307.

Transistors 427 and 437 form a current mirror since the gate and drain of transistor 427 are coupled to the gate of transistor 437. Therefore, the current flowing through transistor 437 is proportional to the current flowing through transistor 427, which is proportional to the positive current. Current source 439 provides a reference current, which is compared to the current that flows through transistor 437. If

the current flowing through transistor 437 rises above the current provided by current source 439, then the voltage at the drain of transistor 437, which is the under-voltage signal 319, goes high. When under-voltage signal 319 goes high and the output of NOR gate 445 will go low, indicating that there is no under-voltage condition.

Transistors 427 and 441 also form a current mirror since the gate and drain of transistor 427 are coupled to the gate of transistor 441. Therefore, the current flowing through transistor 441 is proportional to the current flowing through the transistor 427, which is proportional to the positive current. Current source 443 provides a reference current, which is compared to current that flows through transistor 441. As long as the current flowing through transistor 441 stays below the current provided by current source 443, then the voltage at the drain of transistor 441, which is the over-voltage signal 323, remains low. When over-voltage signal 323 remains low, the output of NOR gate 447 remains high assuming that there was no under-voltage condition indicated by under-voltage signal 319 and no remote off condition indicated by on/off signal 311.

The output of NOR gate 447 is enable/disable signal 331. In one embodiment, enable/disable signal 331 is high if on/off signal 311 is low, or under-voltage signal 319 is high and over-voltage signal 323 is low. Otherwise, enable/disable signal 331 is low.

In one embodiment, the oscillator 467 receives enable/disable signal 331 at the start/stop input 469. In one embodiment, oscillator 467 generates oscillating waveforms at oscillating waveform outputs 471, 473 and 475 while enable/disable signal 331 is high or active. In one embodiment, oscillator 467 does not generate the oscillating waveforms at oscillating waveform outputs 471, 473 and 475 while enable/disable signal 331 is low or in-active. In one embodiment, oscillator 467 begins generating oscillating waveforms starting with new complete cycles on a rising edge of enable/disable signal 331. In one embodiment, oscillator 467 completes existing cycles of the oscillating waveforms generated at oscillating waveform outputs 471, 473 and 475 before stopping the waveforms in response to a falling edge of enable/disable signal 331. That is, oscillator 467 stops generating the waveforms at a point just before the start of an on time of power switch of the next cycle in response to a falling edge of enable/disable signal 331.

In one embodiment, control terminal 145 supplies power to the circuitry of power supply controller 139 and also provides feedback to modulate the duty cycle of switching waveform 335. In one embodiment, control terminal 145 is coupled to the output of the power supply 101 through a feedback circuit to regulate the output voltage of the power supply 101. In one embodiment, an increase in the output voltage of power supply 101 results in the reduction in the duty cycle of switching waveform 335 through feedback received through control terminal 145. Therefore, if the regulation level of the output parameter of power supply 101 that is being controlled, such as output voltage or current or power, is exceeded during operation, additional feedback current is received through control terminal 145. This feedback current flows through resistor 455 and through a shunt regulator formed by transistor 457 and comparator 459. If no feedback current or control terminal current in excess of supply current is received through control terminal 145, the current through transistor 457 is zero. If the current through transistor 457 is zero, and assuming for the time being that there is no current through the diode 451, the current through resistor 479 is zero. If there is no current flowing through resistor 479, then the voltage drop across resistor 479 is zero.

If there is no voltage drop across resistor 479, there is no voltage drop across capacitor 483. As a result, the output of comparator 477 will remain low. If the output of comparator 477 remains low, and assuming for the time being that the output of AND gate 487 remains low, the output of latch 491 will remain high. In this case, the maximum duty cycle signal, which is produced by oscillator waveform output 471, will be generated at the output of AND gate 493. Thus, switching waveform 335 will have the maximum duty cycle produced by oscillator waveform output 471.

Therefore, when the voltage drop across resistor 479 remains at zero, the maximum duty cycle produced at oscillator waveform output 471 is not limited, assuming that the output of AND gate 487 remains low. This is because latch 491 is not reset through the output of comparator 477. However, when the feedback current or control terminal current in excess to the supply current is received through control terminal 145, this feedback current flows through transistor 457. As the amount of current flowing through the transistor 457 increases, the voltage drop across resistor 479 increases correspondingly. As a voltage drop across resistor 479 increases, the voltage drop across capacitor 483 will increase. In any given cycle, when the voltage on the oscillating waveform output 475 crosses below the voltage across the capacitor 483 the output of the comparator will go high and terminate the on-time of the switching waveform 335 or turn off the power switch 495. As a result, the duty cycle (on time as a fraction of the cycle time) of the switching waveform 335 decreases with increase in voltage drop across resistor 479.

In one embodiment, the oscillating waveform at oscillating waveform output 475 is a sawtooth waveform having a duty cycle and period equal to the maximum duty cycle waveform generated at oscillating waveform output 471. As the voltage drop across resistor 479 increases, the output of comparator 477 will go high closer to the beginning of each cycle. When the output of comparator 477 goes high, latch 491 will be reset through NOR gate 489. When latch 491 is reset, the on time of the switching waveform 335 is terminated for that particular cycle and switching waveform 335 remains low for the remainder of that particular cycle. Latch 491 will not be set again until the beginning of the next cycle through switching waveform output 473, assuming that there is a high or active enable/disable signal 331.

Referring now to maximum duty cycle adjuster signal 325, transistor 449 includes a source coupled to control terminal 145 and a gate coupled to the gate and drain of transistor 427 to receive positive current sense signal 307. Transistor 449 and transistor 427 also form a current mirror. Therefore, the current flowing through transistor 449 is proportional to the current flowing through transistor 427, which is proportional to the positive current flowing into multi-function terminal 149. The current that flows through diode 451 is the difference between the current that flows through transistor 449 and the current that flows into current source 453. The current that flows through current source 453 is set such that current will not begin to flow through diode 451 until the current flowing through transistor 449 rises above a threshold. In one embodiment, the above threshold value is chosen such that the maximum duty cycle is not reduced until the positive current flowing into multi-function terminal 149 rises above the threshold used for under-voltage comparison. In one embodiment, the threshold positive current used for under-voltage comparison is approximately 50 microamps and the threshold positive current used for maximum duty cycle adjustment is approximately 60 microamps.

When current begins to flow through diode 451, that current will be combined with current that flows through transistor 457. In one embodiment, the current that flows through diode 451 is maximum duty cycle adjustment signal 327. The current flowing through transistor 457 and diode 451 will flow through resistor 479. As discussed in detail above, current that flows through resistor 479 will result in the voltage drop across resistor 479, which results in a reduction in the maximum duty cycle of switching waveform 335. As the current that flows through resistor 479 increases, the maximum duty cycle of switching waveform 335 will be decreased.

FIG. 5 is a diagram illustrating some of the currents, voltages and duty cycles associated with the power supply controller 139 in accordance with teachings of the present invention. In particular, diagram 501 illustrates when the power supply is enabled in relation to the input current of multi-function terminal 149. The x-axis represents the positive or negative current flowing into or out of multi-function terminal 149. As illustrated, as positive input current rises from zero and crosses over 50 microamps, power supply controller 139 in one embodiment is enabled. At this time, an under-voltage condition is removed. If the current is above 50 microamps but then falls below zero microamps, power supply controller 139 is disabled. At this time, an under-voltage condition is detected. The difference between 50 microamps and zero microamps provides hysteresis, which provides for more stable operation during noise or ripple conditions in the input current.

As the input current rises above 225 microamps, the power supply is disabled. At this time, an over-voltage condition is detected. When the input current falls back below 215 microamps, the power supply is re-enabled. At this time, the over-voltage condition is removed. The difference between 225 microamps and 215 microamps provides hysteresis, which provides for more stable operation during noise or ripple conditions in the input current.

Continuing with diagram 501, when the negative current that flows out from multi-function terminal 149 rises in magnitude to a level above 50 microamps, which is illustrated as -50 microamps in FIG. 5, the power supply is enabled. At this time, the on/off feature of the present invention turns on the power supply. When the negative current falls in magnitude to a level below 40 microamps, which is illustrated as -40 microamps in FIG. 5, the power supply is disabled. At this time, the on/off feature of the present invention turns off the power supply. The difference between -50 microamps and -40 microamps provides hysteresis, which provides for more stable operation during noise or ripple conditions in the input current.

It is worthwhile to note that in one embodiment the positive input current is clamped at 300 microamps and that the negative input current is clamped at 200 microamps. The positive input current would be clamped at 300 microamps when, for example, the multi-function terminal 149 is short-circuited to a supply voltage. The negative input current would be clamped at 200 microamps when, for example, the multi-function terminal is short-circuited to ground.

In diagram 503, the current limit through power switch 147 as adjusted by the present invention is illustrated. Note that the hysteresis of the under-voltage and over-voltage conditions are illustrated from zero microamps to 50 microamps and from 215 microamps to 225 microamps, respectively. In one embodiment, when positive input current is provided into multi-function terminal 149 and there is neither an under-voltage condition nor an over-voltage

condition, the current limit through power switch 147 is 3 amps. However, when negative current flows out from multi-function terminal 149, and the magnitude of the negative current rises above 50 microamps, which is illustrated as -50 microamps in FIG. 5, the current limit through power switch 149 is approximately 1 amp. As the magnitude of the negative current rises to 150 microamps, which is illustrated as -150 microamps in FIG. 5, the current limit through power switch 149 rises proportionally with the negative current to 3 amps. After the magnitude of the negative current rises above 150 microamps, the current limit of the power switch 149 remains fixed at 3 amps. Note that there is also the on/off hysteresis between -50 microamps and -40 microamps in diagram 503.

Diagram 505 illustrates the maximum duty cycle setting of power supply controller 139 in relation to the input current. Note that the hysteresis from -50 microamps to -40 microamps, from zero microamps to 50 microamps and from 215 microamps to 225 microamps as discussed above is included. In the embodiment illustrated in diagram 505, the maximum duty cycle is fixed at 75 percent until a positive input current of 60 microamps is reached. As the input current continues to increase, the maximum duty cycle continues to decrease until an input current of 225 microamps is reached, at which time the maximum duty cycle has been reduced to 33 percent. As illustrated, between 60 microamps and 225 microamps, the maximum duty cycle is inversely proportional to the positive input current. Note that when negative current flows through multi-function terminal 149, and when the power supply is enabled, the maximum duty cycle in one embodiment is fixed at 75 percent.

Diagram 507 illustrates the voltage at multi-function terminal, which is labeled in diagram 507 as line sense voltage, in relation to the input current. When negative current is flowing from multi-function terminal 149, the voltage at multi-function terminal 149 is fixed at the band gap voltage  $V_{BG}$ , which in one embodiment is 1.25 volts. When positive current is flowing into multi-function terminal 149, the voltage at multi-function terminal is fixed at the band gap voltage  $V_{BG}$  plus a threshold voltage  $V_{TP}$ , which in one embodiment sum to 2.3 volts. In the event that a negative current having a magnitude of more than 200 microamps is attempted to be drawn out of the multi-function terminal 149, the voltage at multi-function terminal 149 drops to approximately zero volts. In the event that a positive current of more than 300 microamps flows into multi-function terminal 149, the voltage at multi-function terminal 149 rises. In this case, the voltage will be limited by either by a standard clamp used at the multi-function terminal for the purpose of protection or by the external circuitry driving the multi-function terminal, whichever is lower in voltage.

It is appreciated that the currents, voltages, duty cycle settings and hysteresis settings described in connection with the present invention are given for explanation purposes only and that other values may be selected in accordance with teachings of the present invention. For example, in other embodiments, non hysteretic thresholds may be utilized. Thus the hysteresis values may be greater than or equal to zero.

FIG. 6A is timing diagram illustrating one embodiment of some of the waveforms of a power supply controller in accordance with teachings of the present invention. Referring to both FIGS. 4 and 6A, oscillating waveform output 475 of oscillator 467 generates a sawtooth waveform, which is received by comparator 477. Oscillating waveform output 471 of oscillator 467 generates a maximum duty cycle

signal, which is received by AND gate 493. Enable/disable signal 331, which is received at enable/disable input 469 of oscillator 467, is also illustrated. In FIG. 6A, the enable/disable signal 331 is active. Therefore, the sawtooth waveform of oscillating waveform output 475 and the maximum duty cycle waveform of oscillating waveform output 471 are generated. Note that the sawtooth waveform and the maximum duty cycle waveform have the same frequency and period. One cycle of each of these waveform occurs between time 601 and time 605. The peak of the sawtooth waveform occurs at the same time as the rising edge of the maximum duty cycle waveform. This aspect is illustrated at time 601 and at time 605. The lowest point of the sawtooth waveform occurs at the same time as the falling edge of the maximum duty cycle waveform. This aspect is illustrated at time 603.

Referring now to FIG. 6B, a timing diagram illustrating another embodiment of the waveforms of a power supply controller in accordance with teachings of the present invention is shown. From time 607 to time 609, the enable/disable signal 331 is low or inactive. In one embodiment, a low enable/disable signal 331 disables the power supply. A high or active enable/disable signal 331 enables the power supply. At time 609, the rising edge of enable/disable signal 331 occurs. At this time, oscillating waveform outputs 475 and 471 begin generating the sawtooth waveform and maximum duty cycle waveform, respectively. Note that a new complete cycle of each of these waveforms is generated in response to the rising edge of enable/disable signal 331 at time 609.

From time 609 to time 611, enable/disable signal 331 remains high or active. Thus, during this time, the sawtooth waveform and maximum duty cycle waveform are continuously generated.

At time 611, a falling edge of enable/disable signal 331 occurs. Before oscillator 467 discontinues generating the sawtooth waveform and the maximum duty cycle waveform, the existing cycles of each of these waveforms are allowed to complete. Stated differently, generation of the sawtooth waveform and the maximum duty cycle waveform is discontinued at a point just before the start of the on-time of the switching waveform 335 or the on-time of the power switch of the next cycle. This point in time is illustrated in FIG. 6B at time 613. Note that after time 613, the sawtooth waveform remains inactive at a high value and the maximum duty cycle waveform remains inactive at a low value.

At time 615, another rising edge of enable/disable signal 331 occurs. Therefore, the sawtooth waveform and the maximum duty cycle waveform are generated beginning at a new complete cycle of each waveform. As illustrated in FIG. 6B, a falling edge of enable/disable signal 331 occurs at time 617, which is immediately after the rising edge. However, the sawtooth waveform and maximum duty cycle waveforms are allowed to complete their then existing cycles. This occurs at time 619. After time 619, the waveforms remains inactive as shown during the time between time 619 and time 621, which is when another rising edge of enable/disable signal 331 occurs. At time 621, another new complete cycle of the sawtooth waveform and the maximum duty cycle waveform are generated. Since enable/disable signal 331 is deactivated at time 623, which occurs during a cycle of the sawtooth waveform and the maximum duty cycle waveform, these waveforms are deactivated after fully completing their respective cycles. Thus, by pulsing the on/off control signal at the multi-function terminal it is possible to synchronize the oscillator to the on/off pulse frequency.

FIG. 7 is a schematic of another embodiment of a power supply controller 139 in accordance with the teachings of the



present invention. The power supply controller schematic shown in FIG. 7 is similar to the power supply controller schematic discussed above in FIG. 4. The primary difference between the power supply controller of FIGS. 4 and 7 is that oscillator 467 of FIG. 7 does not have an enable/disable input 469 coupled to receive enable/disable signal 331. As shown in the embodiment depicted in FIG. 7, the enable/disable signal 331 is used to directly gate the switching waveform at the input of AND gate 493. In this embodiment, the oscillator 467 is running all the time and switching waveform 335 will be gated on and off at any point in the cycle in response to the enable/disable signal 331.

To illustrate, FIG. 8 shows one embodiment of timing diagrams of switching waveforms of the power supply controller illustrated in FIG. 7. Referring to both FIGS. 7 and 8, oscillating waveform output 475 of oscillator 467 generates a sawtooth waveform, which is received by comparator 477. Oscillating waveform output 471 of oscillator 467 generates a maximum duty cycle signal, which is received by AND gate 493. Enable/disable signal 331, which is received by AND gate 493, and the output of AND gate 493, which is switching waveform 335, are also illustrated. In FIG. 8, the enable/disable signal 331 is active only some of the time. Therefore, the switching waveform 335 is switching only during those portions of time that the enable/disable signal 331 is active. When the enable/disable signal 331 is not active, switching waveform 335 does not switch.

In the foregoing detailed description, the method and apparatus of the present invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the present invention. The present specification and figures are accordingly to be regarded as illustrative rather than restrictive.

What is claimed is:

1. A power supply controller circuit, comprising:
  - a current input circuit coupled to receive a current for adjusting a current limit of a power switch, the current input circuit to generate a current limit adjustment signal in response to the current; and
  - a control circuit coupled to receive the current limit adjustment signal, the control circuit coupled to adjust the current limit of a current through the power switch in response to the current limit adjustment signal.
2. The power supply controller circuit of claim 1 wherein the power switch is coupled to a primary winding of the power supply.
3. The power supply controller circuit of claim 1 wherein the control circuit is a pulse width modulation circuit that generates a switching waveform coupled to be received by the power switch to regulate a power supply output.
4. The power supply controller of claim 3 wherein the current is representative of a feedback signal from the power supply output, wherein a power supply voltage is regulated through current limit adjustment of the power switch in response to the feedback signal.
5. The power supply controller of claim 3 wherein the control circuit includes a first comparator coupled to compare a voltage representative of the current through the power switch with the current limit adjustment signal such that the power switch is disabled in response to an output of the first comparator when the current limit set by the current limit adjustment signal is exceeded.
6. The power supply controller of claim 5 wherein the control circuit is to generate said switching waveform controlled in response to the output of the first comparator such

that the switching waveform is coupled to limit the current through the power switch.

7. The power supply controller circuit of claim 1 wherein the current limit of the current through the power switch is adjusted by the current when the current limit of the current through the power switch is below a predetermined maximum level.

8. The power supply controller circuit of claim 7 wherein the current limit of the current through the power switch is fixed at the predetermined maximum level for magnitudes of the currents that are higher than the current value corresponding to the predetermined maximum level.

9. The power supply controller of claim 1, wherein the current circuit also generates an enable/disable signal that deactivates the power supply when the magnitude of the current is below an on/off threshold, the on/off threshold having a hysteresis of zero or greater.

10. The power supply controller circuit of claim 9 further comprising an oscillator circuit coupled to an enable/disable signal, the oscillator circuit to start and stop generating a switching waveform in response to the current crossing the on/off threshold.

11. The power supply controller circuit of claim 10 wherein the oscillator circuit is to complete an existing cycle of the switching waveform before the oscillator is to stop generating the switching waveform in response to the enable/disable signal.

12. The power supply controller circuit of claim 10 wherein the oscillator circuit is to start a new complete cycle of the switching waveform if the oscillator circuit is to start generating the switching waveform in response to the enable/disable signal.

13. The power supply controller circuit of claim 1, wherein the current is received by the current input circuit on a low impedance terminal that has a reference voltage with respect to ground.

14. The power supply controller in claim 13, wherein the current limit of the power switch is set by the value of resistance connected between the reference voltage on the low impedance terminal and ground.

15. A method for controlling a power supply, comprising: supplying a first current from a first terminal of a power supply controller;

deactivating the power supply if the first current supplied from the first terminal falls below a first threshold value; and

activating the power supply if the first current supplied from the first terminal rises above a second threshold value.

16. The method of claim 15 wherein deactivating the power supply comprises stopping a switching waveform to control a power switch coupled to a primary winding of the power supply.

17. The method of claim 15 wherein activating the power supply comprises starting a switching waveform to control a power switch coupled to a primary winding of the power supply.

18. The method of claim 17 wherein starting the switching waveform includes starting a new complete cycle of the switching waveform.

19. The method of claim 15 wherein the second threshold value is greater than the first threshold value.

20. The method of claim 15 further comprising limiting the first current supplied from the first terminal to a maximum value.

21. The method of claim 16 wherein stopping the switching waveform includes allowing to complete an existing cycle of the switching waveform.



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22. The method of claim 15 further comprising coupling a switch between the first terminal and ground.

23. The method of claim 15 further comprising coupling a variable resistance between the first terminal and ground.

24. A method for controlling a power supply, comprising:

supplying a first current from a first terminal of a power supply controller;

controlling a second current flowing through a primary winding of the power supply with a power switch coupled to the primary winding; and

adjusting a current limit of the second current in response to the first current.

25. The method of claim 24 wherein adjusting the current limit of the second current comprises increasing the current limit of the second current in response to an increase in the first current.

26. The method of claim 24, wherein adjusting the current limit of the second current comprises decreasing the current limit of the second current in response to a decrease in the first current.

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27. The method of claim 24 further comprising coupling a resistance between the first terminal and ground.

28. The method of claim 24 wherein controlling a second current flowing through the primary winding comprises:

switching the power switch in response to a switching waveform; and

adjusting the switching waveform in response to the first current.

29. The method of claim 28 wherein adjusting the switching waveform comprises:

generating a first voltage in response to the first current;

generating a second voltage in response to the second current; and

adjusting the switching waveform in response to a comparison of the first voltage and the second voltage.

\* \* \* \* \*

1 **GENERAL ALLEGATIONS**

2 9. Power Integrations' products include its TOPSwitch®, TinySwitch®, LinkSwitch®,  
3 and DPA-Switch families of power conversion integrated circuit devices, which are used in power  
4 supplies for electronic devices such as cellular telephones, LCD monitors, and computers. These  
5 products are sold throughout the United States, including California.

6 10. Defendants manufacture power supply controller integrated circuit devices (e.g.,  
7 devices intended for use in power conversion applications such as LCD monitor power supplies,  
8 off-line power supplies or battery chargers for portable electronics), and directly, and through their  
9 affiliates, make, use, import, sell, and offer to sell the same throughout the United States, including  
10 California. Defendants also support and encourage others to import, use, offer for sale, and sell  
11 throughout the United States, including California, products incorporating Defendants' integrated  
12 circuit devices.

13 **FIRST CAUSE OF ACTION**

14 **INFRINGEMENT OF U.S. PATENT NO. 6,351,398**

15 11. The allegations of paragraphs 1-10 are incorporated for this First Cause of Action as  
16 though fully set forth herein.

17 12. Power Integrations is now, and has been since its issuance, the assignee and sole  
18 owner of all right, title, and interest in United States Patent No. 6,351,398, entitled "Method and  
19 Apparatus Providing a Multi-Function Terminal for a Power Supply Controller" ("the '398 patent"),  
20 which was duly and legally issued on February 26, 2002. A true and correct copy of the '398 patent  
21 is attached hereto as Exhibit A.

22 13. On June 28, 2004, Power Integrations filed a complaint for patent infringement  
23 against SG in this District because SG was infringing several Power Integrations patents, including  
24 the '398 patent. Thereafter, Power Integrations filed a similar complaint for patent infringement  
25 with the U.S. International Trade Commission ("ITC") in an effort to obtain expedited relief to  
26 prevent continued infringement through importation of the infringing products into the United  
27 States. The District Court case was stayed pending the proceedings in the ITC. The ITC instituted  
28 an investigation, and a hearing was held before an Administrative Law Judge ("ALJ"), who found





(10) **Number:** US 6,351,398 C1  
(45) **Certificate Issued:** Jul. 28, 2009

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Primary Examiner--My-Trang Ton

(57) **ABSTRACT**

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No. 90/008,364, Dec. 6, 2006

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Filed: Oct. 26, 2000

(62) Division of application No. 09/405,209, filed on Sep. 24, 1999, now Pat. No. 6,462,971.

- (51) **Int. Cl.**  
**H02H 7/122** (2006.01)

- (52) U.S. Cl. .... 363/56.03; 363/49; 363/16

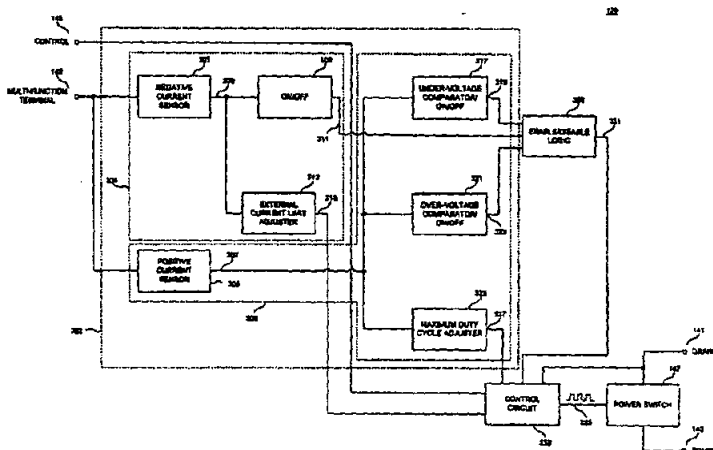
- (58) **Field of Classification Search** ..... None  
See application file for complete search history.

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A power supply controller having a multi-function terminal. In one embodiment, a power supply controller for switched mode power supply includes a drain terminal, a source terminal, a control terminal and a multi-function terminal. The multi-function terminal may be configured in a plurality of ways providing any one or some of a plurality of functions including on/off control, external current limit adjustments, under-voltage detection, over-voltage detection and maximum duty cycle adjustment. The operation of the multi-function terminal varies depending on whether a positive or negative current flows through the multi-function terminal. A short-circuit to ground from the multi-function terminal enables the power supply controller. A short-circuit to a supply voltage from the multi-function terminal disables the power supply controller. The current limit of an internal power switch of the power supply controller may be adjusted by externally setting a negative current from the multi-function terminal. The multi-function terminal may also be coupled to the input DC line voltage of the power supply through a resistance to detect an under-voltage condition, an over-voltage condition and/or adjust the maximum duty cycle of power supply controller. Synchronization of the oscillator of the power supply controller may also be realized by switching the multi-function terminal to power or ground at the desired times.



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1

**EX PARTE  
REEXAMINATION CERTIFICATE  
ISSUED UNDER 35 U.S.C. 307**

THE PATENT IS HEREBY AMENDED AS  
INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN  
DETERMINED THAT:

The patentability of claims 1-14 is confirmed.

Claims 24-29 are cancelled.

2

Claim 15 is determined to be patentable as amended.

Claims 16-23, dependent on an amended claim, are determined to be patentable.

5

15. A method for controlling a power supply, comprising:  
supplying a first current from a first terminal of a power  
supply controller;

10

deactivating the power supply if the first current supplied  
from the first terminal falls below a first threshold  
value; and

15

activating the power supply if the first current supplied  
from the first terminal rises above a second threshold  
value, *wherein the first and second threshold values are  
different.*

\* \* \* \* \*







US006538908B2

(12) **United States Patent**  
Balakrishnan et al.

(10) Patent No.: **US 6,538,908 B2**  
(45) Date of Patent: **Mar. 25, 2003**

(54) **METHOD AND APPARATUS PROVIDING A MULTI-FUNCTION TERMINAL FOR A POWER SUPPLY CONTROLLER**

(75) Inventors: **Balu Balakrishnan**, Saratoga, CA (US);  
**Alex B. Djenguerian**, Saratoga, CA (US); **Leif O. Lund**, San Jose, CA (US)

(73) Assignee: **Power Integrations, Inc.**, San Jose, CA (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 10/167,557

(22) Filed: **Jun. 11, 2002**

(65) **Prior Publication Data**

US 2002/0172055 A1 Nov. 21, 2002

#### Related U.S. Application Data

(63) Continuation of application No. 09/405,209, filed on Sep. 24, 1999, now Pat. No. 6,462,971.

(51) Int. Cl.<sup>7</sup> ..... **H02M 3/24; G05F 5/00**

(52) U.S. Cl. .... **363/95; 363/16; 323/299**

(58) Field of Search ..... **363/16, 20, 19, 363/21.02, 89, 95, 15; 323/282, 283, 284, 285, 351, 299**

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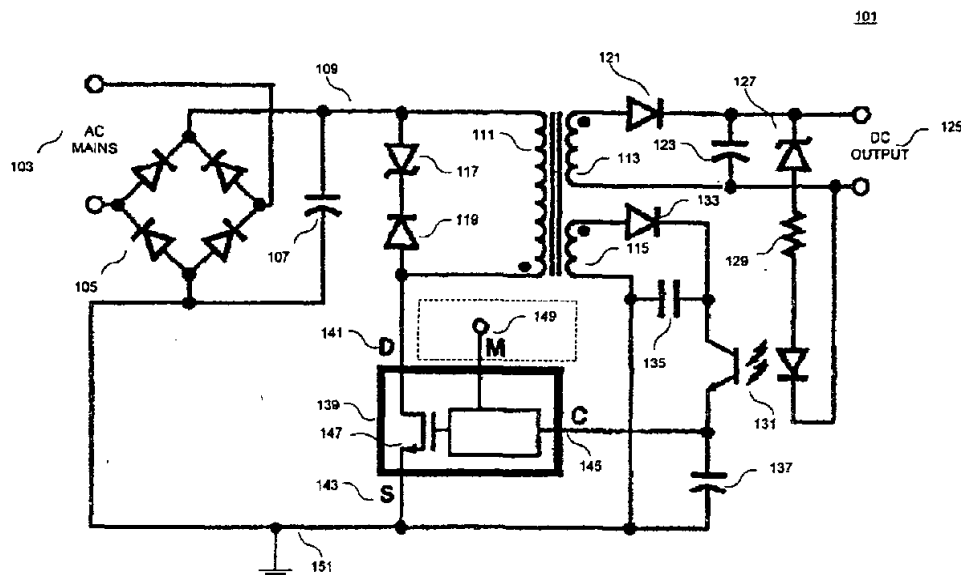
Primary Examiner—Rajnikant B. Patel

(74) Attorney, Agent, or Firm—Blakely Sokoloff Taylor & Zafman, LLP

(57) **ABSTRACT**

A power supply controller having a multi-function terminal. In one embodiment, a power supply controller for switched mode power supply includes a drain terminal, a source terminal, a control terminal and a multi-function terminal. The multi-function terminal may be configured in a plurality of ways providing any one or some of a plurality of functions including on/off control, external current limit adjustments, under-voltage detection, over-voltage detection and maximum duty cycle adjustment. The operation of the multi-function terminal varies depending on whether a positive or negative current flows through the multi-function terminal. A short-circuit to ground from the multi-function terminal enables the power supply controller. A short-circuit to a supply voltage from the multi-function terminal disables the power supply controller. The current limit of an internal power switch of the power supply controller may be adjusted by externally setting a negative current from the multi-function terminal. The multi-function terminal may also be coupled to the input DC line voltage of the power supply through a resistance to detect an under-voltage condition, an over-voltage condition and/or adjust the maximum duty cycle of power supply controller. Synchronization of the oscillator of the power supply controller may also be realized by switching the multi-function terminal to power or ground at the desired times.

34 Claims, 13 Drawing Sheets



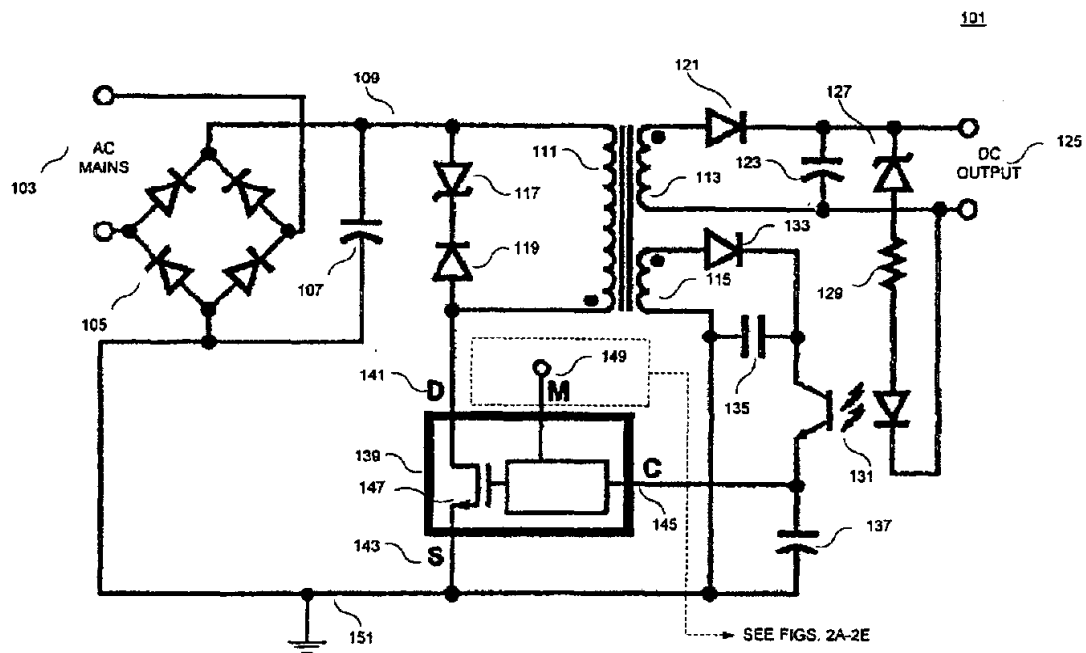


FIG. 1

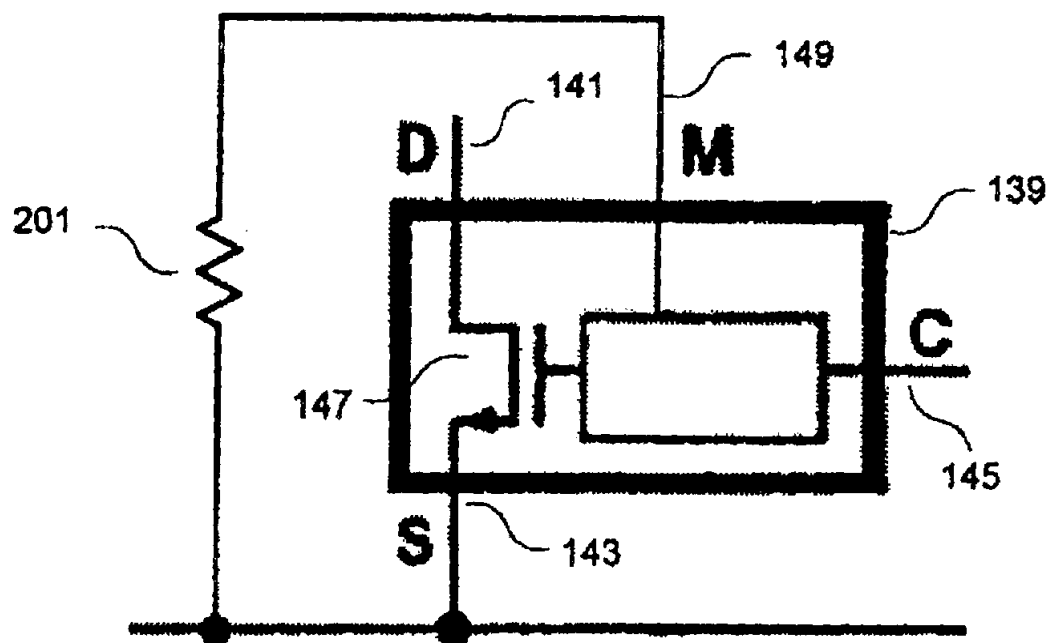


FIG. 2A

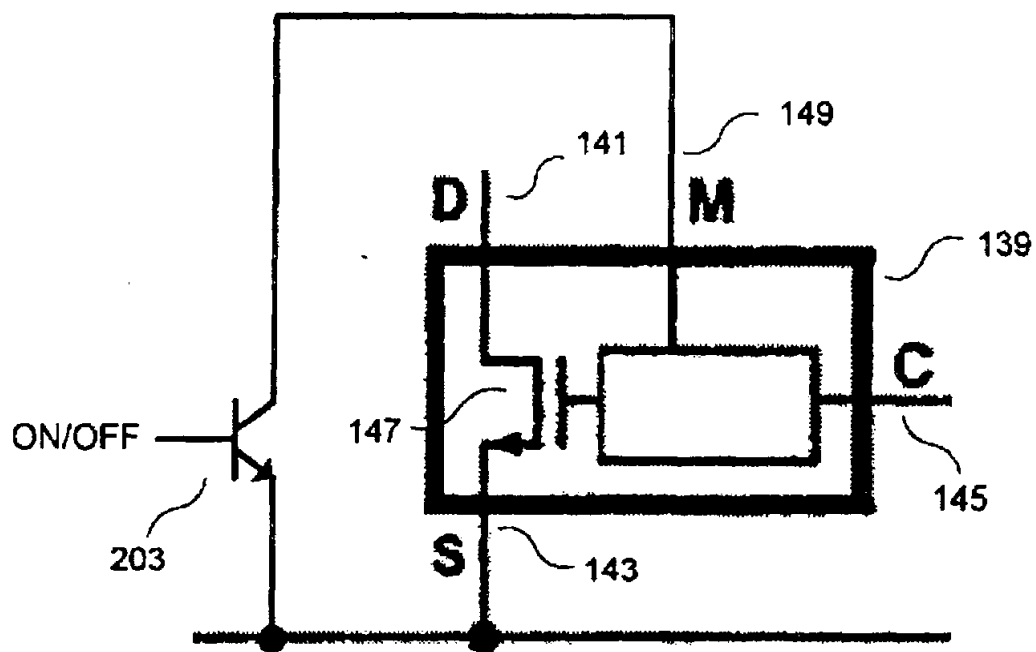


FIG. 2B

all asserted claims of the '398 patent to be valid and infringed and recommended an exclusion order against the infringing SG products. On August 11, 2006, the ITC issued an exclusion order against the infringing SG chips. SG appealed the ITC decision, but the Federal Circuit affirmed the ITC's findings in all respects.

14. After the findings that SG infringed the '398 patent and that the '398 patent was valid in the ITC trial and the issuance of the exclusion order, Fairchild purchased SG. Prior to its purchase of SG, Fairchild was itself also found to have infringed certain other of Power Integrations' patents in a proceeding in the U.S. District Court for the District of Delaware. Like the ITC and the Federal Circuit, the Delaware Jury and Court both rejected Fairchild's challenges to the validity of these other Power Integrations patents as well.

15. Since the acquisition of SG, SG has operated as a wholly-owned subsidiary of Fairchild, and Defendants have continued to sell SG chips and to introduce new chips based on the SG architecture.

16. During the parties' prior litigation, SG initiated multiple challenges to the validity of the '398 patent via filing two separate requests for *ex parte* reexamination before the United States Patent and Trademark Office ("USPTO"), raising a number of allegations of invalidity. On July 28, 2009, the USPTO issued Reexamination Certificate No. 6,351,398 C1, confirming the patentability of claims 1-23 of the '398 patent. A true and correct copy of the '398 Reexamination Certificate is attached hereto as Exhibit B.

17. After the USPTO confirmed the validity of claims in all of the patents previously asserted against SG, Power Integrations contacted Defendants regarding their continued infringement in a letter dated August 10, 2009. Despite the USPTO's confirmation of the validity of the '398 patent and Power Integrations' prior success in proving infringement and validity in the ITC proceeding and on appeal, Defendants have refused to agree to stop infringing Power Integrations' patents.

18. Defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '398 patent in this District and elsewhere by making, using, selling, offering to sell, and/or importing devices, including power supply controller integrated

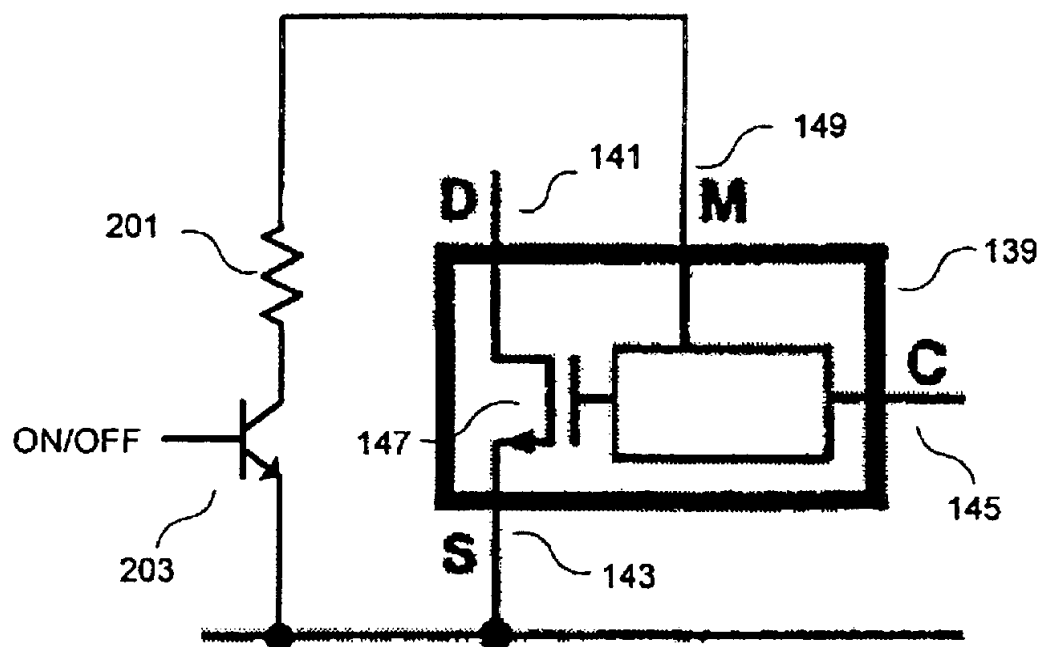


FIG. 2C

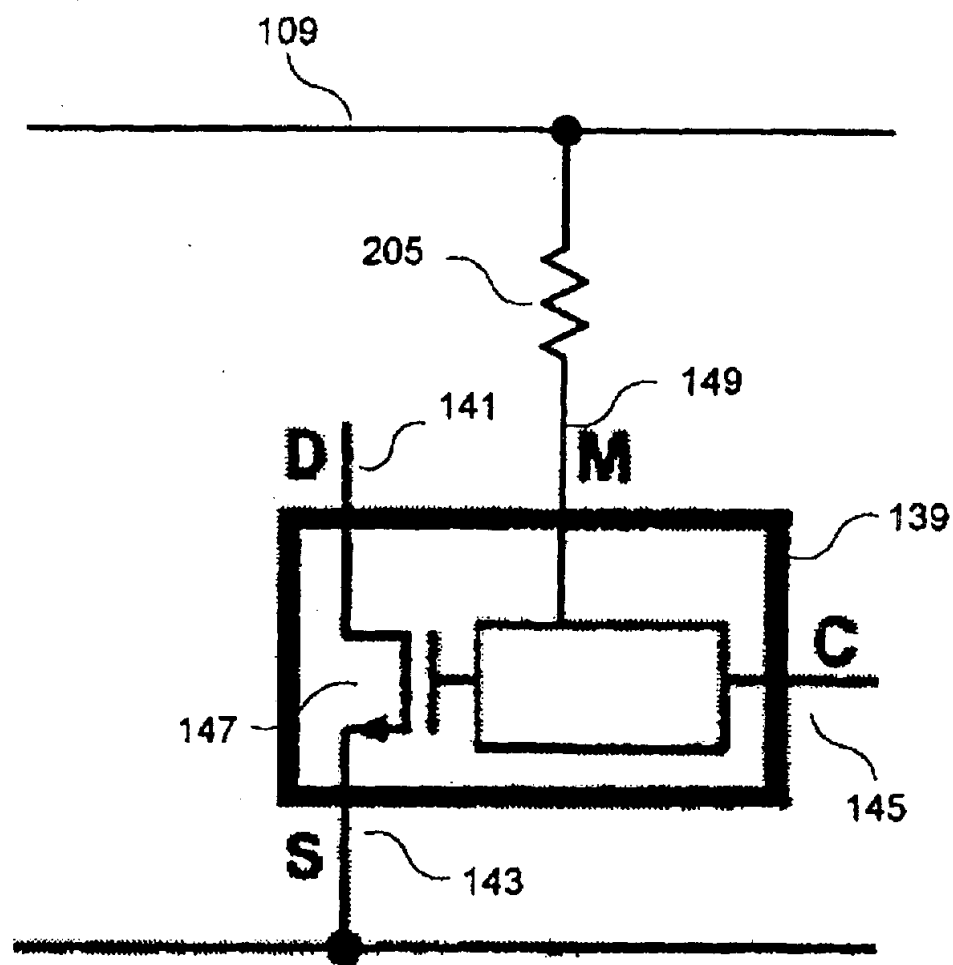


FIG. 2D

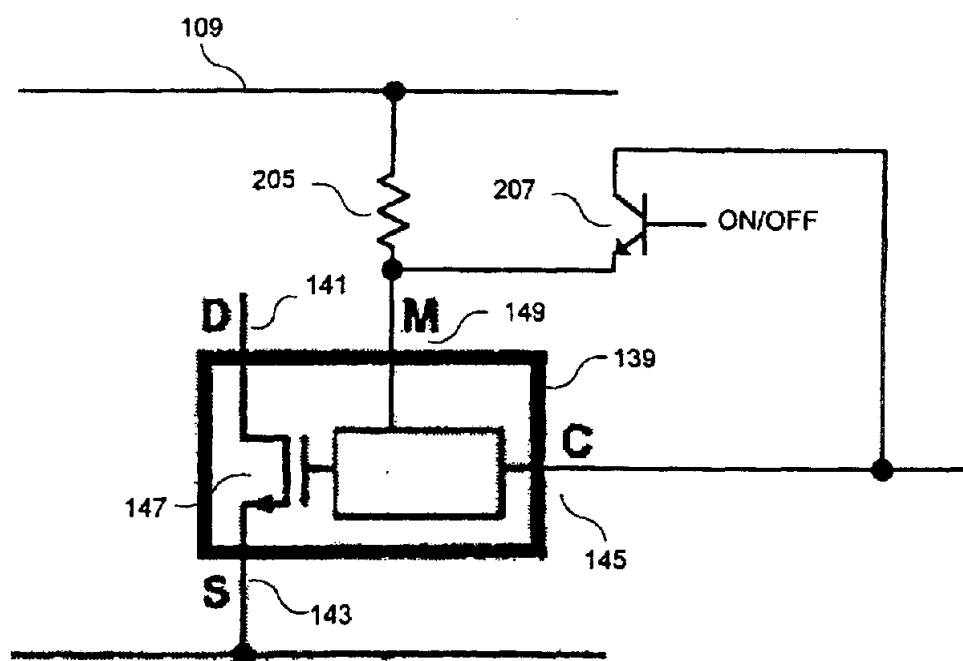


FIG. 2E



FIG. 2F

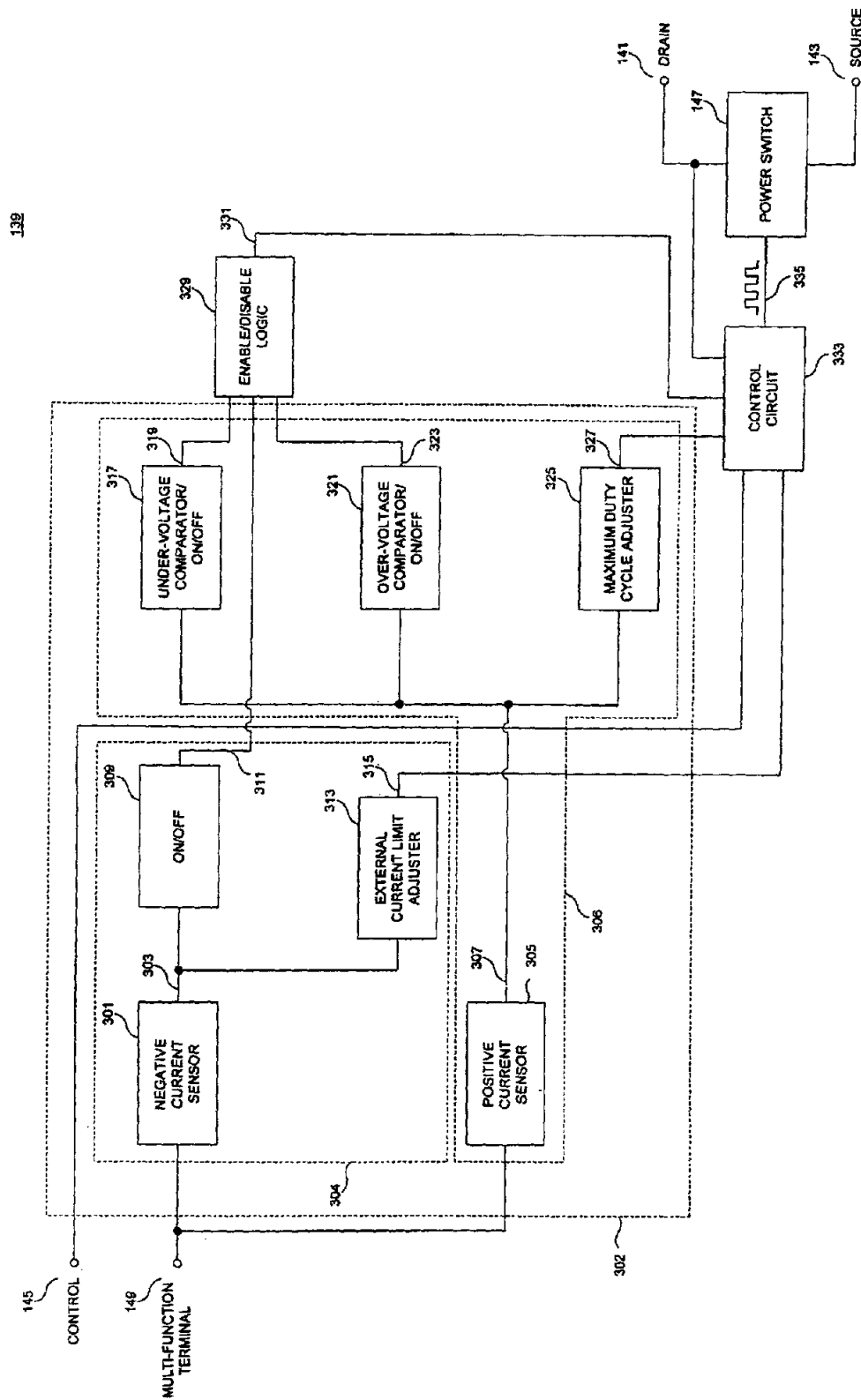


FIG. 3

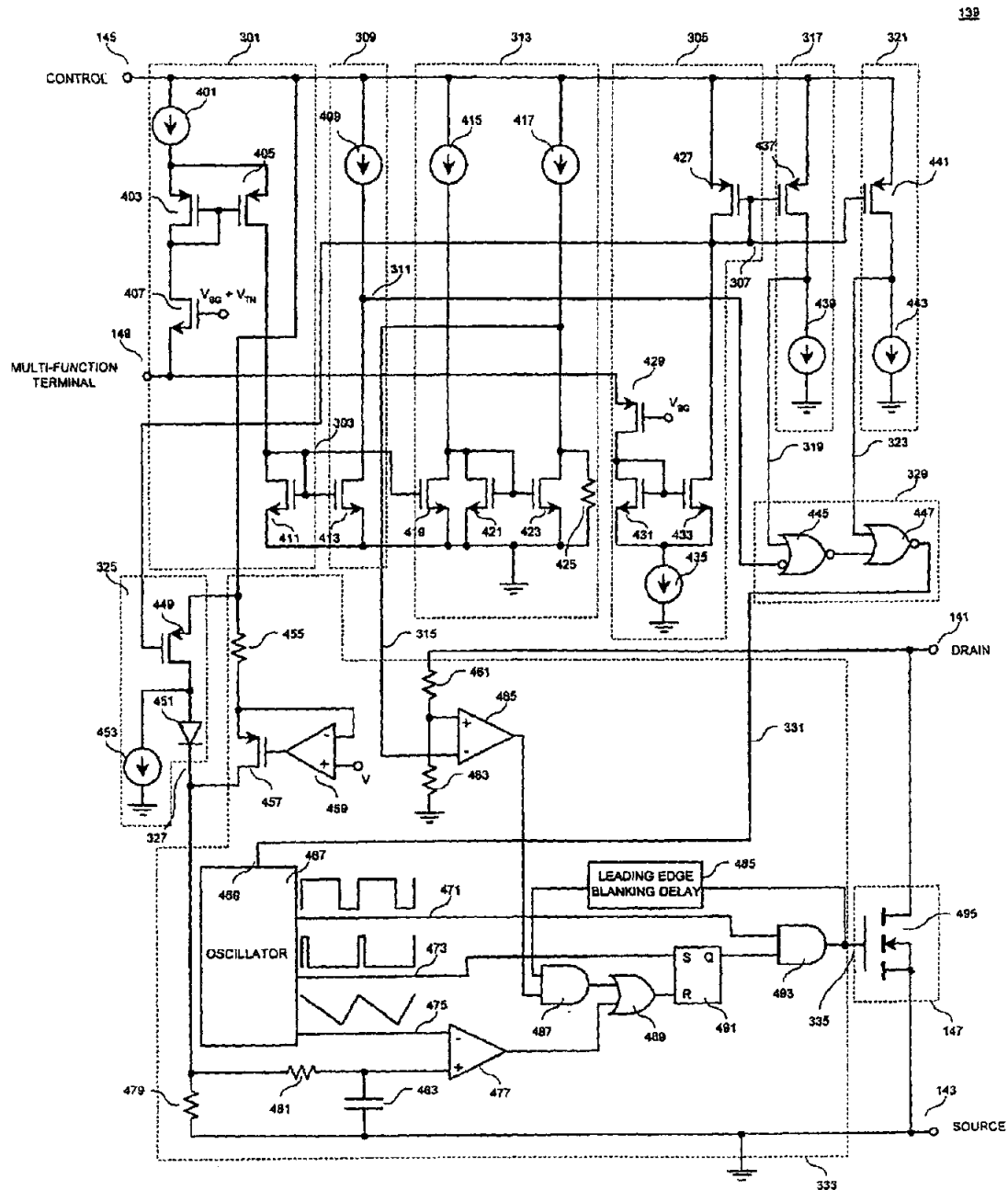


FIG. 4

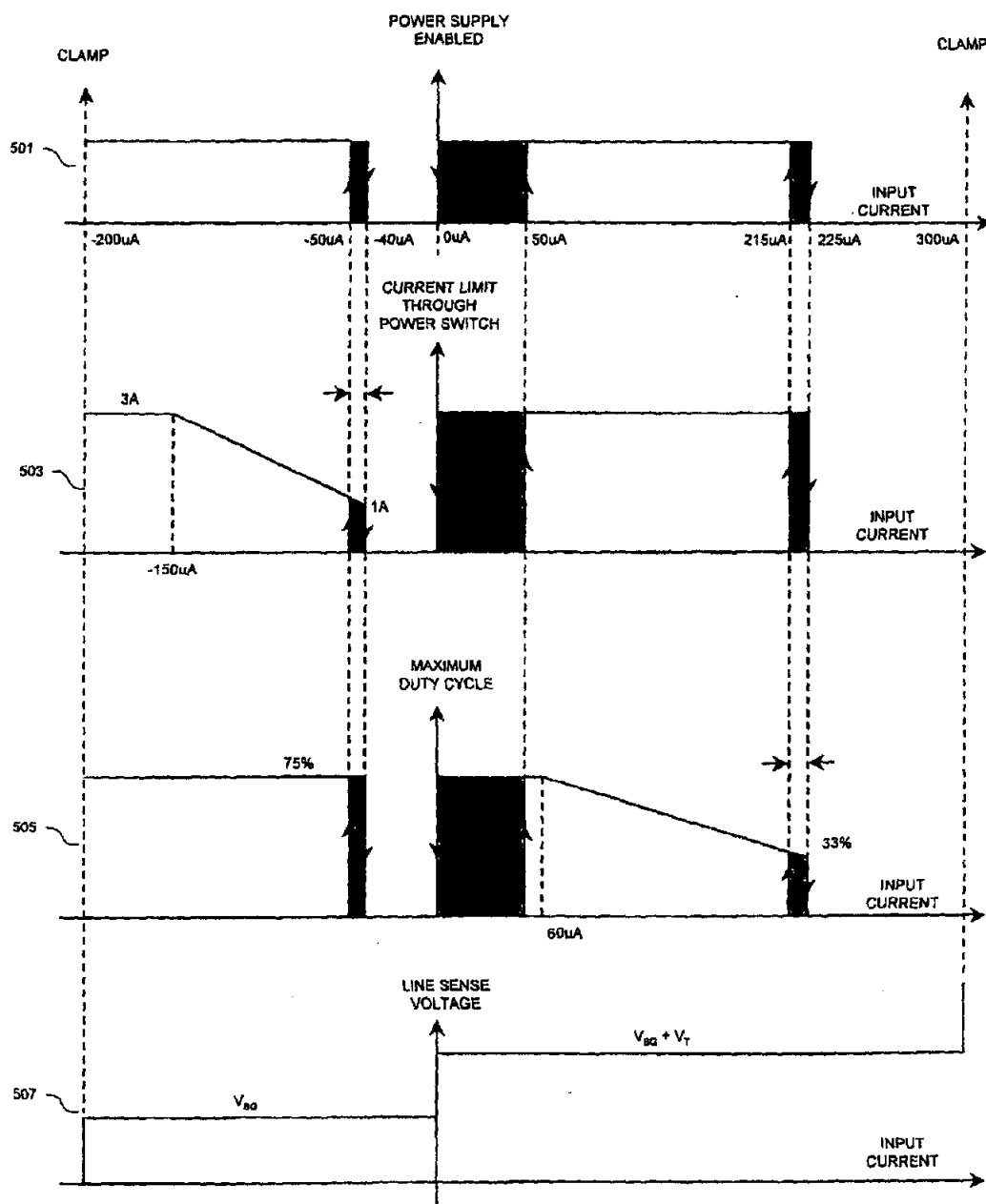


FIG. 5

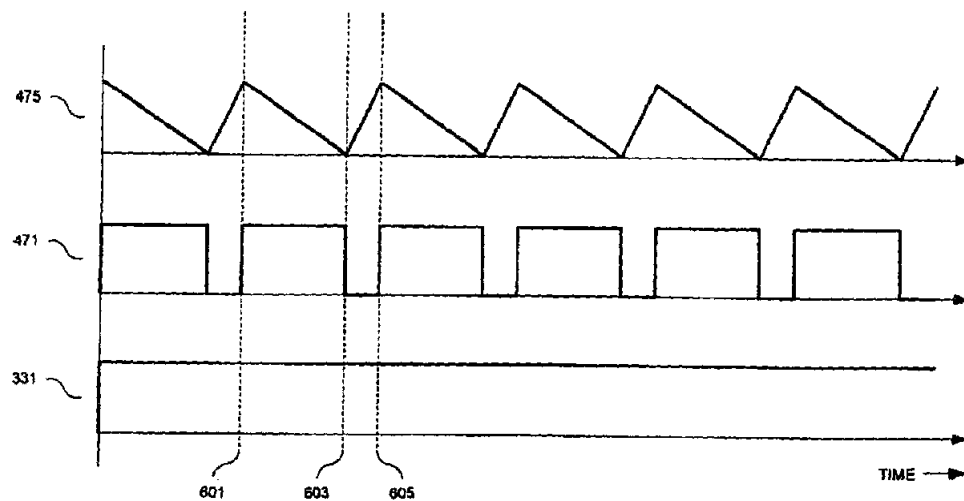


FIG. 6A

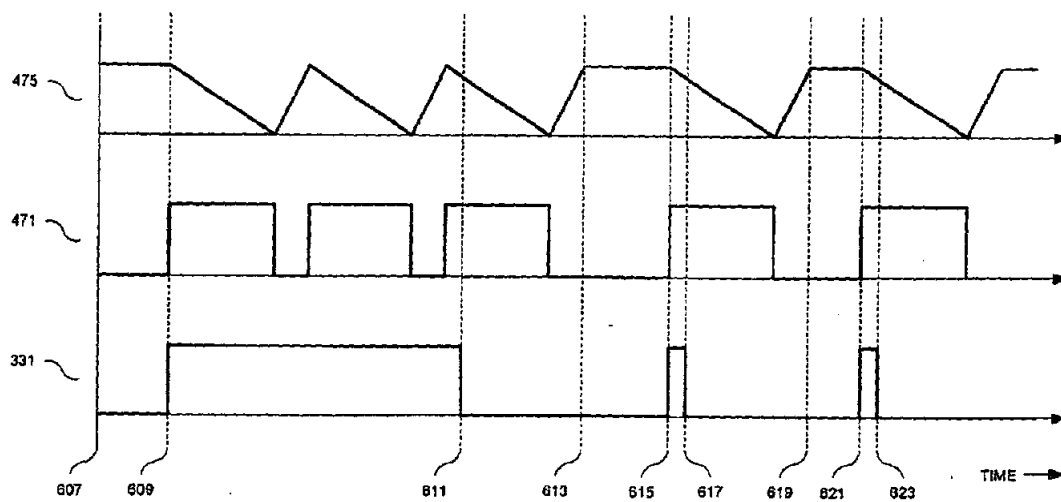


FIG. 6B

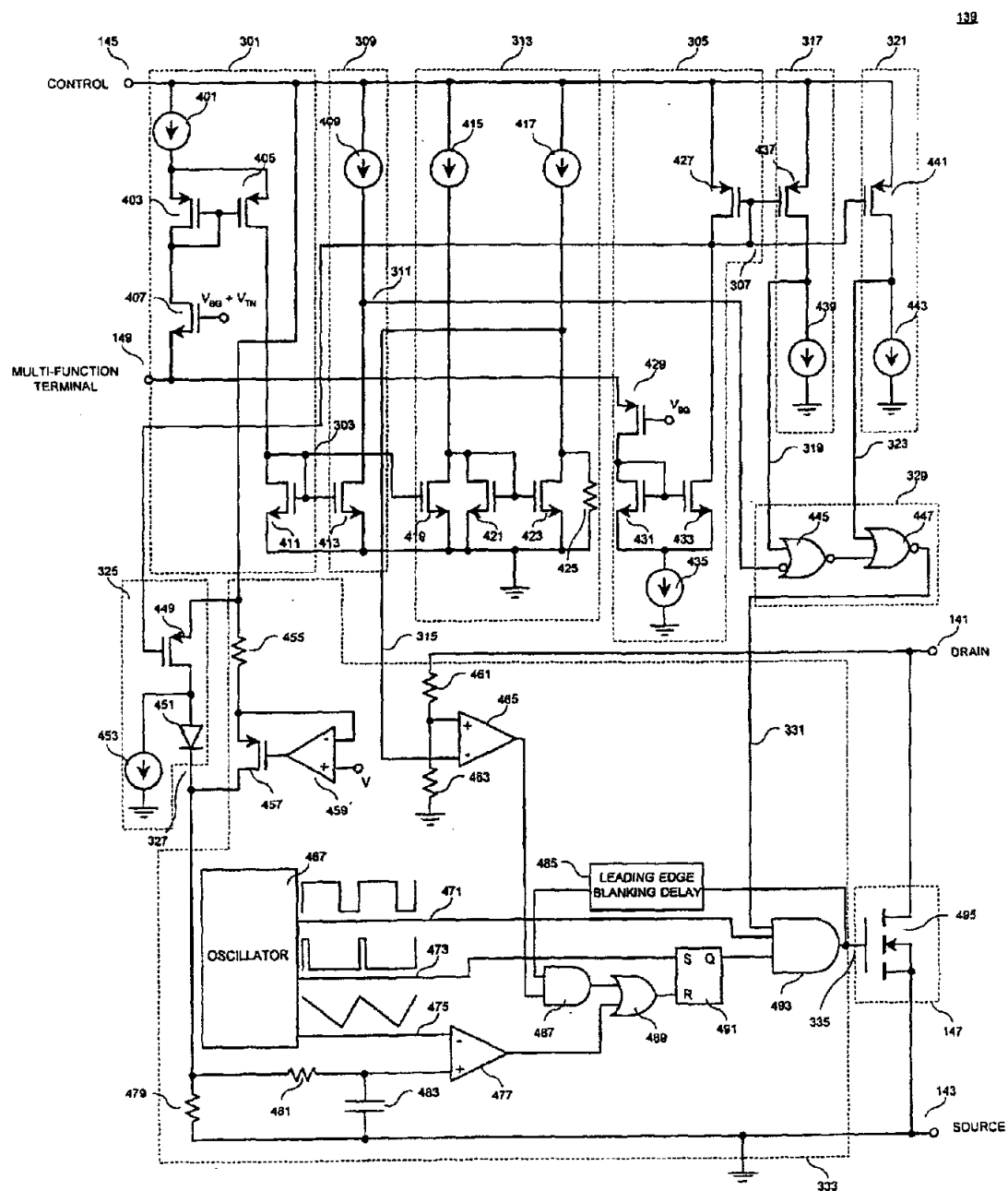


FIG. 7

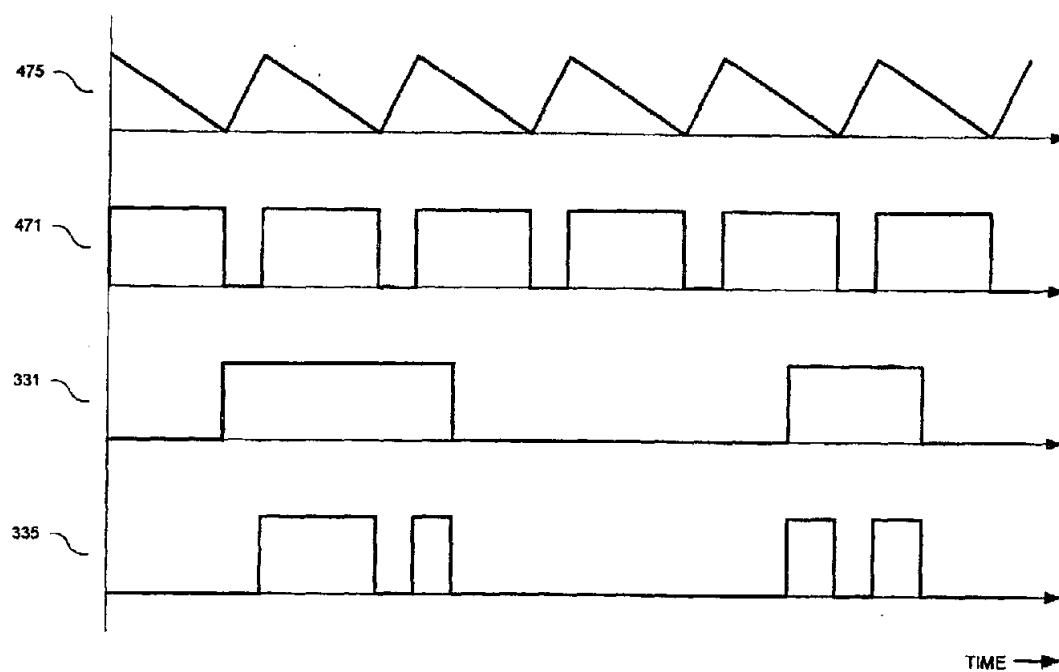


FIG. 8

1 circuit devices, covered by one or more claims of the '398 patent, and/or contributing to or inducing  
2 the same by third-parties, all to the injury of Power Integrations. In particular, Defendants' power  
3 supply controller products that include what Defendants characterize as providing "Constant Output  
4 Power Limit" functionality by sensing line voltage variations through sensing current at an input pin  
5 of the controller infringe Power Integrations' '398 patent.

6 19. Defendants' acts of infringement have injured and damaged Power Integrations.

7 20. Defendants' acts of infringement have been, and continue to be, willful so as to  
8 warrant the enhancement of damages awarded as a result of their infringement. In particular,  
9 despite Power Integrations' prior notice of infringement as early as 2004, despite the prior  
10 determinations of infringement and validity by the ITC and the subsequent affirmance of those  
11 determinations by the Court of Appeals for the Federal Circuit, despite the '398 patent emerging  
12 from reexamination, and despite Power Integrations' renewed notice to Defendants of their  
13 infringement, Defendants have failed to commit to ceasing all infringement of the '398 patent.

14 21. Defendants' infringement has caused irreparable injury to Power Integrations and  
15 will continue to cause irreparable injury until Defendants are enjoined from further infringement by  
16 this Court.

## 17 **SECOND CAUSE OF ACTION**

### 18 **INFRINGEMENT OF U.S. PATENT NO. 6,538,908**

19 22. The allegations of paragraphs 1-10 are incorporated for this Second Cause of Action  
20 as though fully set forth herein.

21 23. Power Integrations is now, and has been since its issuance, the assignee and sole  
22 owner of all right, title, and interest in United States Patent No. 6,538,908, entitled "Method and  
23 Apparatus Providing a Multi-Function Terminal for a Power Supply Controller" ("the '908 patent"),  
24 which was duly and legally issued on March 25, 2003. A true and correct copy of the '908 patent is  
25 attached hereto as Exhibit C.

26 24. On June 28, 2004, Power Integrations filed a complaint for patent infringement  
27 against SG in this District because SG was infringing several Power Integrations patents, including  
28 the '908 patent. Thereafter, Power Integrations filed a similar complaint for patent infringement



1

# METHOD AND APPARATUS PROVIDING A MULTI-FUNCTION TERMINAL FOR A POWER SUPPLY CONTROLLER

This is a Continuation of U.S. application Ser. No. 09/405,209, filed Sep. 24, 1999, now U.S. Pat. No. 6,462,971.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates generally to power supplies and, more specifically, the present invention relates to a switched mode power supply controller.

### 2. Background Information

Electronic devices use power to operate. Switched mode power supplies are commonly used due to their high efficiency and good output regulation to power many of today's electronic devices. In a known switched mode power supply, a low frequency (e.g. 50 Hz or 60 Hz mains frequency), high voltage alternating current (AC) is converted to high voltage direct current (DC) with a diode rectifier and capacitor. The high voltage DC is then converted to high frequency (e.g. 30 to 300 kHz) AC, using a switched mode power supply control circuit. This high frequency, high voltage AC is applied to a transformer to transform the voltage, usually to a lower voltage, and to provide safety isolation. The output of the transformer is rectified to provide a regulated DC output, which may be used to power an electronic device. The switched mode power supply control circuit provides usually output regulation by sensing the output controlling it in a closed loop.

A switched mode power supply may include an integrated circuit power supply controller coupled in series with a primary winding of the transformer. Energy is transferred to a secondary winding from the primary winding in a manner controlled by the power supply controller to provide the clean and steady source of power at the DC output. The transformer of a switched mode power supply may also include another winding called a bias or feedback winding. The bias winding provides the operating power for the power supply controller and in some cases it also provides a feedback or control signal to the power supply controller. In some switched mode power supplies, the feedback or control signal can come through an opto-coupler from a sense circuit coupled to the DC output. The feedback or control signal may be used to modulate a duty cycle of a switching waveform generated by the power supply controller or may be used to disable some of the cycles of the switching waveform generated by the power supply controller to control the DC output voltage.

A power supply designer may desire to configure the power supply controller of a switched mode power supply in a variety of different ways, depending on for example the particular application and/or operating conditions. For instance, there may be one application in which the power supply designer would like the power supply controller to have one particular functionality and there may be another application in which the power supply designer would like the power supply controller to have another particular functionality. It would be convenient for power supply designer to be able to use the same integrated power supply controller for these different functions.

In order to provide the specific functions to the power supply controller, additional pins or electrical terminals are added for each function to the integrated circuit power supply controllers. Consequently, each additional function

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generally translates into an additional pin on the power supply controller chip, which translates into increased costs and additional external components. Another consequence of providing additional functionality to power supply controllers is that there is sometimes a substantial increase in power consumption by providing the additional functionality.

## SUMMARY OF THE INVENTION

Power supply controller methods and apparatuses are disclosed. In one embodiment, a power supply controller circuit is described including a current input circuit coupled to receive a current. In one embodiment, the current input circuit is to generate an enable/disable signal in response to the current. The power supply controller is to activate and deactivate the power supply in response to the enable/disable signal. In another embodiment, a current limit of a power switch of the power supply controller is adjusted in response to the current. In yet another embodiment, a maximum duty cycle of the power switch of the power supply is adjusted in response to the current. Additional features and benefits of the present invention will become apparent from the detailed description, figures and claims set forth below.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention detailed illustrated by way of example and not limitation in the accompanying figures.

FIG. 1 is a schematic illustrating one embodiment of a power supply including a power supply controller having a multi-function terminal in accordance with the teachings of the present invention.

FIG. 2A is a schematic illustrating one embodiment of a power supply controller having a multi-function terminal configured to limit the current of the power switch in the power supply controller to a desired value in accordance with the teachings of the present invention.

FIG. 2B is a schematic illustrating one embodiment of a power supply having a multi-function terminal configured to provide a switchable on/off control to the power supply in accordance with the teachings of the present invention.

FIG. 2C is a schematic illustrating one embodiment of the power supply having a multi-function terminal configured to limit the current of the power switch in the power supply controller to a desired value and provide a switchable on/off control to the power supply controller in accordance with the teachings of the present invention.

FIG. 2D is a schematic illustrating one embodiment of a power supply having a multi-function terminal configured to provide line under-voltage detection, line over-voltage detection and maximum duty cycle reduction of the power supply in accordance with the teachings of the present invention.

FIG. 2E is a schematic illustrating one embodiment of a power supply having a multi-function terminal configured to provide line under-voltage detection, line over-voltage detection, maximum duty cycle reduction and a switchable on/off control to the power supply in accordance with the teachings of the present invention.

FIG. 2F is a schematic illustrating one embodiment of current mode control of a power supply controller having a multi-function terminal configured to regulate the current limit of the power switch in response to the power supply output in accordance with the teachings of the present invention.

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FIG. 3 is a block diagram illustrating one embodiment of a power supply controller including a multi-function terminal in accordance with teachings of the present invention.

FIG. 4 is a schematic illustrating one embodiment of a power supply controller including a multi-function terminal in accordance with the teachings of the present invention.

FIG. 5 is a diagram illustrating one embodiment of currents, voltages and duty cycles in relation to current through a multi-function terminal of a power supply controller in accordance with teachings of the present invention.

FIG. 6A is a diagram illustrating one embodiment of timing diagrams of switching waveforms of a power supply controller including a multi-function terminal in accordance with teachings of the present invention.

FIG. 6B is a diagram illustrating another embodiment of timing diagrams of switching waveforms of the power supply controller including a multi-function terminal in accordance with teachings of the present invention.

FIG. 7 is a schematic illustrating another embodiment of a power supply controller including a multi-function terminal in accordance with the teachings of the present invention.

FIG. 8 is a diagram illustrating another embodiment of timing diagrams of switching waveforms of the power supply controller including a multi-function terminal in accordance with teachings of the present invention.

#### DETAILED DESCRIPTION

A method and an apparatus providing a multi-function terminal in a power supply controller is disclosed. In the following description, numerous specifically details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific detail need not be employed to practice the present invention. In other instances, well-known materials or methods have not been described in detail in order to avoid obscuring the present invention.

In one embodiment of the present invention, a power supply controller is provided with the functionality of being able to remotely turn on and off the power supply. In another embodiment, the power supply controller is provided with the functionality of being able to externally set the current limit of a power switch in the power supply controller, which makes it easier to prevent saturation of the transformer reducing transformer size and cost. Externally settable current limit also allows the maximum power output to be kept constant over a wide input range reducing the cost of components that would otherwise have to handle the excessive power at high input voltages. In yet another embodiment, the power supply controller is provided with the functionality of being able to detect an under-voltage condition in the input line voltage of the power supply so that the power supply can be shutdown gracefully without any glitches on the output. In still another embodiment, the power supply controller is provided with the functionality of being able to detect an over-voltage condition in the input line voltage of the power supply so that the power supply can be shut down under this abnormal condition. This allows the power supply to handle much higher surge voltages due to the absence of reflected voltage and switching transients on the power switch in the power supply controller. In another embodiment, the power supply controller is provided with the functionality of being able to limit the maximum duty cycle of a switching waveform generated by a power supply controller to control the DC output of the

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power supply. In so doing, saturation of the transformer during power up is reduced and the excess power capability at high input voltages is safely limited. Increased duty cycle at low DC input voltages also allows for smaller input filter capacitance. Thus, this feature results in cost savings on many components in the power supply including the transformer. In yet another embodiment, some or all of the above functions are provided with a single multi-function terminal in the power supply controller. That is, in one embodiment, a plurality of additional functions are provided to power supply controller without the consequence of adding a corresponding plurality of additional terminals or pins to the integrated circuit package of the power supply controller. In one embodiment, one or some of the above functions are available when positive current flows into the multi-function terminal. In another embodiment, one or some of the above functions are available when negative current flows out from the multi-function terminal. In one embodiment, the voltage at the multi-function terminal is fixed at a particular value depending on whether positive current flows into the multi-function terminal or whether negative current flows out from the multi-function terminal.

The multi-function features listed above not only save cost of many components and improve power supply performance but also, they save many components that would otherwise be required if these features were implemented externally.

FIG. 1 is a block diagram illustrating one embodiment of a power supply 101 including a power supply controller 139 having a multi-function terminal 149 in accordance with the teachings of the present invention. As illustrated, power supply 101 includes an AC mains input 103, which is configured to receive an AC voltage input. A diode rectifier 105 is coupled to AC mains input to rectify the AC voltage. Capacitor 107 is coupled to diode rectifier 105 to convert the rectified AC into a steady DC line voltage 109, which is coupled to a primary winding 111 of a transformer. Zener diode 117 and diode 119 are coupled across primary winding 111 to provide clamp circuitry.

As illustrated in FIG. 1, primary winding 111 is coupled to a drain terminal 141 of power supply controller 139. Power supply controller 139 includes a power switch 147 coupled between the drain terminal 141 and a source terminal 143, which is coupled to ground. When power switch 147 is turned on, current flows through primary winding 111 of the transformer. When current flows through primary winding 111, energy is stored in the transformer. When power switch 147 is turned off, current does not flow through primary winding 111 and the energy stored in the transformer is transferred to secondary winding 113 and bias winding 115.

A DC output voltage is produced at DC output 125 through diode 121 and capacitor 123. Zener diode 127, resistor 129 and opto-coupler 131 form feedback circuitry or regulator circuitry to produce a feedback signal received at a control terminal 145 of the power supply controller 139. The feedback or control signal is used to regulate or control the voltage at DC output 125. As the voltage across DC output 125 rises above a threshold voltage determined by Zener diode 127, resistor 129 and opto-coupler 131, additional feedback current flows into control terminal 145. In one embodiment, control terminal 145 also provides a supply voltage for circuitry of power supply controller 139 through bias winding 115, diode 133, capacitor 135 and capacitor 137.

As shown in FIG. 1, power supply controller 139 includes a multi-function terminal 149, which in one embodiment

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enables power supply controller 139 to provide one or a plurality of different functions, depending on how multi-function terminal 149 is configured. Some examples of how multi-function terminal 149 may be configured are shown in FIGS. 2A through 2F.

For instance, FIG. 2A is a diagram illustrating one embodiment of a power supply controller 139 including a resistor 201 coupled between the multi-function terminal 149 and the source terminal 143. In one embodiment, the source terminal 143 is coupled to ground. In one embodiment, the voltage at multi-function terminal 149 is fixed when negative current flows from multi-function terminal 149. In one embodiment, the negative current that flows through resistor 201 is used to set externally the current limit of power switch 147. Thus, the power supply designer can choose a particular resistance for resistor 201 to set externally the current limit of power switch 147. In one embodiment, resistor 201 may be a variable resistor, a binary weighted chain of resistors or the like. In such embodiment, the current limit of power switch 147 may be adjusted externally by varying the resistance of resistor 201. In one embodiment, the current limit of power switch 147 is directly proportional to the negative current flowing through resistor 201.

FIG. 2B is a diagram illustrating another embodiment of a power supply controller 139 including a switch 203 coupled between multi-function terminal 149 and source terminal 143. In one embodiment, source terminal 143 is coupled to ground. In one embodiment, power supply controller 139 switches power switch 147 when multi-function terminal 149 is coupled to ground through switch 203. In one embodiment, power supply controller 139 does not switch power switch 147 when multi-function terminal 149 is disconnected from ground through switch 203. In particular, when an adequate amount of negative current flows from multi-function terminal 149, power supply 101 is enabled. When substantially no current flows from multi-function terminal 149, power supply 101 is disabled. In one embodiment, the amount of current that flows from multi-function terminal 149 to ground through switch 203 is limited. Thus, in one embodiment, even if multi-function terminal 149 is short-circuited to ground through switch 203, the amount of current flowing from multi-function terminal 149 to ground is limited to a safe amount.

FIG. 2C is a diagram illustrating yet another embodiment of a power supply controller 139 including resistor 201 and switch 203 coupled in series between multi-function terminal 149 and source terminal 143, which in one embodiment is ground. The configuration illustrated in FIG. 2C combines the functions illustrated and described in connection with FIGS. 2A and 2B above. That is, the configuration illustrated in FIG. 2C illustrates a power supply controller 139 having external adjustment of the current limit of power switch 147, through the selection of the resistance for resistor 201, and on/off functionality through switch 203. When switch 203 is on, power supply controller 139 will switch power switch 147 with a current limit set by resistor 201. When switch 203 is off, power supply controller 139 will not switch power switch 147 and power supply 101 will be disabled.

FIG. 2D is a diagram illustrating still another embodiment of a power supply controller 139 including a resistor 205 coupled between the line voltage 109 and multi-function terminal 149. Referring briefly back to FIG. 1 above, DC line voltage 109 is generated at capacitor 107 and is input to the primary winding 111 of the transformer of power supply 101. Referring back the FIG. 2D, in one embodiment, multi-function terminal 149 is substantially fixed at a par-

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ticular voltage when positive current flows into multi-function terminal 149. Therefore, the amount of positive current flowing through resistor 205 into multi-function terminal 149 is representative of line voltage 109, which is input to the primary winding 111. Since the positive current flowing through resistor 205 into multi-function terminal 149 represents the line voltage 109, power supply controller 139 can use this positive current to sense an under-voltage condition in line voltage 109 in one embodiment. An under-voltage condition exists when the line voltage 109 is below a particular under-voltage threshold value. In one embodiment, if a line under-voltage condition is detected, power switch 147 is not switched by power supply controller 139 until the under-voltage condition is removed.

In one embodiment, power supply controller 139 can use the positive current flowing through resistor 205 into multi-function terminal 149 to detect an over-voltage condition in line voltage 109. An over-voltage condition when line voltage 109 rises above a particular over-voltage threshold value. In one embodiment, if a line over-voltage condition is detected, power switch 147 is not switched by power supply controller 139 until the over-voltage condition is removed.

In one embodiment, power supply controller 139 can also use the positive current flowing through resistor 205 and multi-function terminal 149 to detect for increases or decreases in line voltage 109. As line voltage 109 increases, for a given fixed maximum duty cycle, the maximum power available to secondary winding 113 in power supply 101 of FIG. 1 usually increases. As line voltage 109 decreases, less power is available to secondary winding 113 in power supply 101. In most cases, the excess power available at the DC output 125 is undesirable under overload conditions due to high currents that need to be handled by components. In some instances, it is also desirable to increase the maximum power available to DC output 125 at low input DC voltages to save on cost of the input filter capacitor 107. Higher duty cycle at low DC input voltage allows lower input voltage operation for a given output power. This allows larger ripple voltage on capacitor 107, which translates to a lower value capacitor. Therefore, in one embodiment, power supply controller 139 adjusts the maximum duty cycle of a switching waveform used to control or regulate power switch 147 in response to increases or decreases in line voltage 109. In one embodiment, the maximum duty cycle of the switching waveform used to control power switch 147 is inversely proportional to the line voltage 109. As mentioned earlier, reducing the duty cycle with increasing input DC voltage has many advantages. For instance, it reduces the value and hence the cost of capacitor 107. In addition, it limits excess power at high line voltages reducing the cost of the clamp circuit (117, 119), the transformer and the output rectifier 121 due to reduced maximum power ratings on these components.

It is appreciated that since only a single resistor 201 to ground, or a single resistor 205 to line voltage 109, is utilized for implementing some of the functions of power supply controller 139, a power savings is realized. For instance, if a resistor divider were to be coupled between power and ground, and a voltage output of the resistor divider coupled to a terminal of power supply controller 139 were to be used, current would continuously flow through both the resistor divider and into a sensor terminal of the power supply controller. This would result in increased power consumption. However in one embodiment of the power supply controller 139, only the single resistor 201 to ground or single resistor 205 to line voltage 109 is utilized, thereby eliminating the need for a current to flow through both the resistor divider and into power supply controller 139.

FIG. 2E is a diagram illustrating yet another embodiment of a power supply controller 139 including resistor 205, as described above, coupled between the line voltage 109 and multi-function terminal 149. FIG. 2E also includes a switch 207 coupled between control terminal 145 and multi-function terminal 149. In one embodiment, resistor 205 provides the same functionality as discussed above in connection with FIG. 2D. Therefore, when switch 207 is switched off, the configuration illustrated in FIG. 2E is identical to the configuration described above in connection with FIG. 2D.

In one embodiment, control terminal 145 provides a supply voltage for power supply controller 139 in addition to providing a feedback or control signal to power supply controller 139 from DC output 125. As a result, in one embodiment, switch 207 provides in effect a switchable low resistance connection between a supply voltage (control terminal 145) and multi-function terminal 149. In one embodiment, the maximum positive current that can flow into multi-function terminal 149 is limited. Therefore, in one embodiment, even when switch 207 provides, in effect, a short-circuit connection from a supply voltage, the positive current that flows into multi-function terminal 149 is limited to a safe amount. However, in one embodiment, the positive current that does flow through switch 207, when activated, into multi-function terminal 149 triggers an over-voltage condition. As discussed above, power supply 139 discontinues switching power switch 147 during an over-voltage condition until the condition is removed. Therefore, switch 207 provides on/off functionality for power supply controller 139. When switch 207 is activated, the low resistance path to control terminal 145 is removed and the positive current flowing into multi-function terminal 149 is limited to the current that flows from line voltage 109 through resistor 205. Assuming that neither an under-voltage condition nor an over-voltage condition exists, power supply controller 139 will resume switching power switch 147, thereby re-enabling power supply 101.

FIG. 2F is a diagram illustrating another embodiment of a power supply controller 139 using current mode control to regulate the current limit of the power supply. As shown, resistor 201 is coupled between the multi-function terminal 149 and the source terminal 143 and the transistor 209 of an opto-coupler coupled between multi-function terminal 149 and a bias supply, such as for example control terminal 145. Similar to FIG. 2A, the negative current that flows out from multi-function terminal 149 is used to set externally the current limit of power switch 147. In the embodiment illustrated in Figure in FIG. 2F, the current limit adjustment function can be used for controlling the power supply output by feeding a feedback signal from the output of the power supply into multi-function terminal 149. In the embodiment depicted in FIG. 2F, the current limit is adjusted in a closed loop to regulate the output of the power supply (known as current mode control) by adding the opto-coupler output between multi-function terminal 149 and the bias supply.

In one embodiment, the power supply controller configurations described in connection with FIGS. 2A through 2F all utilize the same multi-function terminal 149. Stated differently, in one embodiment, the same power supply controller 139 may be utilized in all of the configurations described. Thus, the presently described power controller 139 provides a power supply designer with added flexibility. As a result, a power supply designer may implement more than one of the above functions at the same time using the presently described power supply controller 139. In addition, the same functionality may be implemented in

more than one way. For example, power supply 101 can be remotely turned on and off using either power or ground. In particular, the power supply 101 can be turned on and off by switching to and from the control terminal (supply terminal for the power supply controller) using the over-voltage detection feature, or by switching to and from ground using the on/off circuitry.

FIGS. 2A through 2F provide just a few examples of use of the multi-function terminal. A person skilled in the art will find many other configurations for use of the multifunction pin. The uses for the multi-function terminal, are therefore, not limited to the few examples shown.

It is worthwhile to note that different functions of the presently described power supply controller 139 may be utilized at different times during different modes of operation of power supply controller 139. For instance, some features may be implemented during startup operation, other functions may be implemented during normal operation, while still other functions may be implemented during standby operation. Indeed, it is appreciated that a power supply designer may implement other circuit configurations to use with a power supply controller 139 in accordance with teachings of the present invention. The configurations illustrated in FIGS. 2A through 2F are provided simply for explanation purposes.

FIG. 3 is a block diagram illustrating one embodiment of a power supply controller 139 in accordance with teachings of the present invention. As shown in the embodiment illustrated, power supply controller 139 includes a current input circuit 302, which in one embodiment serves as multi-function circuitry. In one embodiment, current input circuit 302 includes a negative current input circuit 304 and a positive current input circuit 306. In one embodiment, negative current input circuit 304 includes negative current sensor 301, on/off circuitry 309 and external current limit adjuster 313. In one embodiment, positive current input circuit 306 includes positive current sensor 305, under-voltage comparator 317, over-voltage comparator 321 and maximum duty cycle adjuster 325.

As shown in FIG. 3, negative current sensor 301 and positive current sensor 305 are coupled to multi-function terminal 149. In one embodiment, negative current sensor 301 generates a negative current sense signal 303 and positive current sensor generates a positive current sense signal 307. For purposes of this description, a negative current may be interpreted as current that flows out of multi-function terminal 149. Positive current may be interpreted as current that flows into multi-function terminal 149. In one embodiment, on/off circuitry 309 is coupled to receive negative current sense signal 303. External current limit adjuster 313 is coupled to receive negative current sense signal 303.

In one embodiment, under-voltage comparator 317 is coupled to receive positive current sense signal 307. Over-voltage comparator 321 is coupled to receive positive current sense signal 307. As discussed earlier, both under-voltage and over-voltage comparators also function as on/off circuits. Maximum duty cycle adjuster 325 is also coupled to receive positive current sense signal 307.

In one embodiment, on/off circuitry 309 generates an on/off signal 311, under-voltage comparator 317 generates an under-voltage signal 319 an over-voltage comparator 321 generates an over-voltage signal 323. As shown in the embodiment illustrated in FIG. 3, enable/disable logic 329 is coupled to receive the on/off signal 311, the under-voltage

signal 319 and the over-voltage signal 323. The under-voltage and over-voltage signals can also be used for on/off functions as noted earlier.

In one embodiment, enable/disable logic 329 generates an enable/disable signal 331, which is coupled to be received by control circuit 333. The control circuit 333 is also coupled to receive a control signal from control terminal 145. In addition, control circuit 333 is also coupled to receive a drain signal from drain terminal 141, a maximum duty cycle adjustment signal 327 from maximum duty cycle adjuster 325 and an external current limit adjustment signal 315 from external current limit adjuster 313.

In one embodiment, control circuit 333 generates a switching waveforms 335, which is coupled to be received by power switch 147. In one embodiment, power switch 147 is coupled between drain terminal 141 and source terminal 143 to control a current flowing through the primary winding 111 of power supply 101, which is coupled to drain terminal 141.

In one embodiment, negative current sensor 301 senses current that flows out of negative current sensor 301 through multi-function terminal 149. Negative current sense signal 303 is generated in response to the current that flows from negative current sensor 301 through multi-function terminal 149. In one embodiment, current that flows from negative current sensor 301 through multi-function terminal 149 typically flows through an external resistance or switch coupled between multi-function terminal 149 and ground.

In one embodiment, positive current sensor 305 senses current that flows into positive current sensor 305 through multi-function terminal 149. Positive current sense signal 307 is generated in response to the current that flows into positive current sensor 305 through multi-function terminal 149. In one embodiment, current that flows into positive current sensor 305 through multi-function terminal 149 typically flows through an external resistance coupled between multi-function terminal 149 and the DC line voltage 109 input to the primary winding 111 of a power supply 101 and/or another voltage source. In another embodiment the current flows through an external resistance or a switch coupled between the multi-function terminal 149 and another voltage source. In one embodiment, the line voltage 109 input to primary winding 111 is typically a rectified and filtered AC mains signal.

As mentioned above, in one embodiment, positive current does not flow while negative current flows, and vice versa. In one embodiment, the negative current sensor 301 and positive current sensor 305 are designed in such a way that they are not active at the same time. Stated differently, negative current sense signal 303 is not active at the same time as positive current sense signal 307 in one embodiment.

In one embodiment, the voltage at multi-function terminal 149 is fixed at a first level when negative current flows out of power supply controller 139 from multi-function terminal 149. In one embodiment, the first level is selected to be approximately 1.25 volts. In one embodiment, the voltage at multi-function terminal 149 is fixed at a second level when positive current flows into power supply controller 139 through multi-function terminal 149. In one embodiment, the second level is selected to be approximately 2.3 volts.

In one embodiment, on/off circuitry 309 generates on/off signal 311 in response to negative current sense signal 303. In one embodiment, when the current flowing from multi-function terminal 149 through an external resistance to ground is less than a predetermined on/off threshold level, on/off circuitry 309 generates on/off signal 311 to switch off

the power supply 101. In one embodiment, when the current flowing from multi-function terminal 149 is greater than a predetermined on/off threshold level, on/off circuitry 309 generates on/off signal 311 to switch on the power supply 101. In one embodiment, the magnitude of the on/off threshold level is approximately 40 to 50 microamps, including hysteresis.

In one embodiment, external current limit adjuster 313 generates external current limit adjustment signal 315 in response to negative current sense signal 303. In one embodiment, when the magnitude of the negative current flowing from multi-function terminal 149 through an external resistance or switch to ground is below a predetermined level, the current limit adjuster 313 generates an external current limit adjustment signal to limit the current flowing through power switch 147. In one embodiment, when the magnitude of the negative current flowing from multi-function terminal 149 is below a predetermined level, the current flowing through power switch 147 is limited to an amount directly proportional to the current flowing out of power supply controller 139 from multi-function terminal 149. In one embodiment, predetermined level is approximately 150 microamps. In one embodiment, if the magnitude of the negative current flowing out of power supply controller 139 from multi-function terminal 149 is greater than the predetermined level, the current flowing through power switch 147 is internally limited or clamped to a fixed safe maximum level. Therefore, the current flowing through power switch 147 is clamped to a safe value, even when multi-function terminal 149 is shorted to ground. In one embodiment, the current flowing through power switch 147 is internally limited or clamped to value of 3 amps.

In one embodiment, since the voltage at multi-function terminal 149 is fixed at a particular voltage when current flows out of power supply controller 139 through multi-function terminal 149, the current limit through power switch 147 can be accurately set externally with a single large value, low-cost, resistor externally coupled between multi-function terminal 149 and ground. By using a large external resistance, the current flowing from multi-function terminal 149 is relatively small. As mentioned above, the current flowing from multi-function terminal 149 in one embodiment is in the microamp range. Since the current flowing from multi-function terminal 149 is relatively small, the amount of power dissipated is also relatively small.

In one embodiment, multi-function terminal 149 is coupled to the DC line voltage 109 input to the primary winding 111 through an external resistance. In one embodiment, the amount of current flowing into multi-function terminal 149 represents the DC input line voltage to the power supply 101. In one embodiment, under-voltage comparator 317 generates under-voltage signal 319 in response to the resulting positive current sense signal 307. In one embodiment, when the current flowing into multi-function terminal 149 rises above a first predetermined threshold, under-voltage comparator 317 generates under-voltage signal 319 to enable the power supply. In one embodiment, when the current flowing into multi-function terminal 149 falls below a second predetermined threshold, under-voltage comparator 317 generates under-voltage signal 319 to disable the power supply. In one embodiment, the first predetermined threshold is greater than the second predetermined threshold to provide hysteresis. By providing hysteresis or a hysteretic threshold, unwanted switching on and off of the power supply 101 resulting from noise or ripple is reduced. In one embodiment, the first predetermined threshold is approximately 50 microamps and the

second predetermined threshold is approximately 0 microamps. In another embodiment, a hysteretic threshold is not utilized. Thus the hysteresis is greater than or equal to zero.

In one embodiment, over-voltage comparator 321 generates over-voltage signal 323 in response to the positive current sense signal 307. In one embodiment, when the current flowing into multi-function terminal 149 rises above a third predetermined threshold, over-voltage comparator 321 generates over-voltage signal 323 to disable the power supply. In one embodiment, when the current flowing into multi-function terminal 149 falls below a fourth predetermined threshold, over-voltage comparator 321 generates over-voltage signal 323 to enable the power supply. In one embodiment, the third predetermined threshold is greater than the fourth predetermined threshold to provide hysteresis. By providing hysteresis or a hysteretic threshold, unwanted switching on and off of the power supply resulting from noise is reduced. In one embodiment, the third predetermined threshold is approximately 225 microamps and the fourth predetermined threshold is approximately 215 microamps. In one embodiment, the third and fourth predetermined thresholds are selected to be approximately four to five times greater than the first predetermined threshold discussed above for an AC mains input 103 of approximately 85 volts to 265 volts AC. In another embodiment, a hysteretic threshold is not utilized. Thus the hysteresis is greater than or equal to zero.

In one embodiment, power switch 147 is able to tolerate higher voltages when not switching. When the power supply is disabled, power switch 147 does not switch. Therefore, it is appreciated that over-voltage comparator 321 helps to protect the power supply 101 from unwanted input power surges by disabling the power switch 147.

In one embodiment, over-voltage and under-voltage comparators 321 and 317 may also be used for on/off functionality, similar to on/off circuitry 309. In particular, multi-function terminal 149 may be switchably coupled to a on/off control signal source to provide a positive current that flows into multi-function terminal 149 that cross the under-voltage or over-voltage thresholds (going above the third or below the fourth predetermined thresholds). For example, when the positive current through the multi-function pin crosses above the first predetermined threshold of the under-voltage comparator 317, the power supply will be enabled and when the positive current goes below the second predetermined threshold of the under-voltage comparator 317, the power supply is disabled. Similarly, when the positive current through the multi-function pin crosses above the third predetermined threshold of the over-voltage comparator 321, the power supply will be disabled and when the positive current goes below the fourth predetermined threshold of the over-voltage comparator 321, the power supply is enabled.

In one embodiment, maximum duty cycle adjuster 325 generates maximum duty cycle adjustment signal 327 in response to the positive current sense signal 307. In one embodiment, maximum duty cycle adjustment signal 327, which is received by control circuit 333, is used to adjust the maximum duty cycle of the switching waveform 335 used to control power switch 147. In one embodiment, the maximum duty cycle determines how long a power switch 147 can be on during each cycle. For example, if the maximum duty cycle is 50 percent, the power switch 147 can be on for a maximum of 50 percent of each cycle.

Referring briefly for example to the power supply 101 of FIG. 1, while power switch 147 is on, power is stored in the

transformer core through the primary winding 111. While the power switch 147 is off, power is delivered from the transformer core to the secondary winding of the transformer in power supply 101. To delivery a given power level, for a lower DC input voltage 109, a higher duty cycle is required and for a higher DC input voltage 109, a lower duty cycle is required. In one embodiment of the present invention, maximum duty cycle adjuster 325 decreases the maximum duty cycle of power switch 147 in response to increases in the DC input voltage 109. In one embodiment, maximum duty cycle adjuster 325 increases the maximum duty cycle of power switch 147 in response to decreases in the DC input voltage 109. Stated differently, the maximum duty cycle is adjusted to be inversely proportional to the current that flows into multi-function terminal 149 in one embodiment of the present invention.

Referring back to FIG. 3, in one embodiment, the maximum duty cycle is adjusted within a range of 33 percent to 75 percent based on the amount of positive current that flows into multi-function terminal 149. In one embodiment, maximum duty cycle adjuster 325 does not begin to decrease the maximum duty cycle until the amount of current that flows into multi-function terminal 149 rises above a threshold value. In one embodiment, that threshold value is approximately 60 microamps. In one embodiment, the maximum duty cycle is not adjusted if negative current flows out of multi-function terminal 149. In this case, the maximum duty cycle is fixed at 75 percent in one embodiment of the present invention.

In one embodiment, enable/disable logic 329 receives as input on/off signal 311, under-voltage signal 319 and over-voltage signal 323. In one embodiment, if any one of the under-voltage or over-voltage conditions exist, enable/disable logic 329 disables power supply 101. In one embodiment, when the under-voltage and over-voltage conditions are removed, enable/disable logic 329 enables power supply 101. In one embodiment, power supply 101 may be enabled or disabled by starting and stopping, respectively, the switching waveform 335 at the beginning of a switching cycle just before the power switch is to be turned on. In one embodiment, enable/disable logic 329 generates enable/disable signal 331, which is received by the oscillator in the control circuit 333 to start or stop the oscillator at the beginning of a switching cycle of switching waveform 335. When enabled the oscillator will start a new on cycle of the switching waveform. When disabled the oscillator will complete the current switching cycle and stop just before the beginning of the next cycle.

In one embodiment, control circuit 333 generates switching waveform 335 to control power switch 147 in response to a current sense signal received from drain terminal 141, enable/disable signal 331, maximum duty cycle adjustment signal 327, a control signal from control terminal 145 and external current limit adjustment signal 315.

In one embodiment, the enable/disable signal can also be used to synchronize the oscillator in the control circuit to an external on/off control signal source having a frequency less than that of the oscillator. The on/off control signal can be input to the multi-function terminal through any of the three paths that generate the enable/disable signal: on/off circuitry 309, under-voltage comparator 317 or over-voltage comparator 321. As discussed, enable/disable the oscillator in the control circuit 333, in one embodiment, begins a new complete cycle of switching waveform at 335 using known techniques in response to enable/disable signal 331, which represents the on/off control signal at the multi-function input. By turning the on/off control signal "on" at the

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multi-function input for a fraction of the switching cycle and then "off," the oscillator is enabled to start a new complete cycle. Therefore, if the external on/off control signal has short "on" pulses at a frequency less than the oscillator in the control circuit, the oscillator will produce a switching cycle each time an on pulse is detected, thus providing a switching waveform that is synchronized to the external frequency.

In an alternate embodiment shown below in FIG. 7, the enable/disable signal 331 directly disables or turns off the power switch through the AND gate 493 when an under-voltage or over-voltage condition exists. In this embodiment, the power switch can be enabled or disabled in the middle of a cycle and consequently, synchronization of the switching waveform through a on/off control signal at the multi-function input is not provided.

FIG. 4 is a schematic of one embodiment of a power supply controller 139 in accordance with the teachings of the present invention. As illustrated, negative current sensor 301 includes a current source 401 coupled to control terminal 145. Transistors 403 and 405 form a current mirror coupled to current source 401. In particular, transistor 403 has a source coupled to current source 401 and a gate and drain coupled to the gate of transistor 405. The source of transistor 405 is also coupled to current source 401. Transistor 407 is coupled between the drain and gate of transistor 403 and multi-function terminal 149. In one embodiment, the gate of transistor 407 is coupled to a band gap voltage  $V_{BG}$  plus a threshold voltage  $V_{TN}$ . In one embodiment,  $V_{BG}$  is approximately 1.25 volts,  $V_{TN}$  is approximately 1.05 volts and  $V_{BG}+V_{TN}$  is approximately 2.3 volts. Transistors 411 and 413 also form a current mirror coupled to the drain of transistor 405. In particular, the gate and drain of transistor 411 are coupled to the drain of transistor 405 and the gate of transistor 413. In one embodiment, negative current sense signal 303 is generated at the gate and drain of transistor 411. The sources of transistors 411 and 413 are coupled to ground. In one embodiment, ground is provided through source terminal 143.

In one embodiment, on/off circuitry 309 includes a current source 409 coupled between the drain of transistor 413 and control terminal 145. In one embodiment, on/off signal 311 is generated at the drain of transistor 413.

In one embodiment, external current limit adjuster 313 includes a current source 415 coupled between control terminal 145 and the drain of transistor 419 and the gate and drain of transistor 421. The source of transistor 419 and the source of transistor 421 are coupled to ground. The gate of transistor 419 is coupled to receive negative current sense signal 303. External current limit adjuster 313 also includes a current source 417 coupled between control terminal 145 and the drain of transistor 423 and resistor 425. The source of transistor 423 and resistor 425 are coupled to ground. External current limit adjustment signal 315 is generated at the drain of transistor 423.

In one embodiment, positive current sensor 305 includes transistor 429 having a source coupled to multi-function terminal 149 and the current mirror formed with transistors 431 and 433. In particular, transistor 431 has a gate and drain coupled to the drain of transistor 429 and the gate of transistor 433. Current source 435 is coupled between ground and the sources of transistors 431 and 433. The gate of transistor 429 is coupled to band gap voltage  $V_{BG}$ . The drain of transistor 433 is coupled to the current mirror formed with transistors 427 and 437. In particular, the gate and drain of transistor 427 are coupled to the gate of transistor 437 and the drain of transistor 433. The sources of

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transistors 427 and 437 are coupled to control terminal 145. Positive current sense signal 307 is generated at the gate and drain of transistor 427.

In one embodiment, under-voltage comparator 317 includes a current source 439 coupled between the drain of transistor 437 and ground. Under-voltage signal 319 is generated at the drain of transistor 437.

In one embodiment, over-voltage comparator 321 includes a current source 443 coupled between the drain of transistor 441 and ground. Transistor 441 has a source coupled to control terminal 145 and a gate coupled to receive positive current sense signal 307. Over-voltage signal 323 is generated at the drain of transistor 441.

In one embodiment, enable/disable logic 329 includes NOR gate 445 having an input coupled to receive under-voltage signal 319 and an inverted input coupled to receive on/off signal 311. Enable/disable logic 329 also includes NOR gate 447 having an input coupled to receive over-voltage signal 323 and an input coupled to an output of NOR gate 445. Enable/disable signal 331 is generated at the output of NOR gate 447.

In one embodiment, maximum duty cycle adjuster 325 includes a transistor 449 having a source coupled to control terminal 145 and a gate coupled to receive positive current sense signal 307. Maximum duty cycle adjuster 325 also includes a current source 453 coupled between the drain of transistor 449 and ground. A diode 451 is coupled to the drain of transistor 449 to produce maximum duty cycle adjustment signal 327.

In one embodiment, power switch 147 includes a power metal oxide semiconductor field effect transistor (MOSFET) 495 coupled between drain terminal 141 and source terminal 143. Power MOSFET 495 has a gate coupled to receive a switching waveform 335 generated by pulse width modulator 333.

In one embodiment, control circuit 333 includes a resistor 455 coupled to the control terminal 145. A transistor 457 has a source coupled to resistor 455 and a negative input of a comparator 459. A positive input of comparator 459 is coupled to a voltage  $V$ , which in one embodiment is approximately 5.7 volts. An output of comparator 459 is coupled to the gate of transistor 457. The drain of transistor 457 is coupled to diode 451 and resistor 479. The other end resistor 479 is coupled to ground. A filter is coupled across resistor 479. The filter includes a resistor 481 coupled to resistor 479 and capacitor 483 coupled to resistor 481 and ground. Capacitor 483 is coupled to a positive input of comparator 477.

In one embodiment, control circuit 333 is a pulse width modulator, which has an oscillator 467 with three oscillating waveform outputs 471, 473 and 475. Oscillator 467 also includes an enable/disable input 469 coupled to receive enable/disable signal 331. In one embodiment, control circuit 333 also includes a voltage divider including resistors 461 and 463 coupled between drain terminal 141 and ground. A node between resistors 461 and 463 is coupled to a positive input of a comparator 465. A negative input of comparator 465 is coupled to receive external current limit adjustment signal 315.

In one embodiment, oscillating waveform output 471 is coupled to a first input of AND gate 493. Oscillating waveform output 473 is coupled to a set input of latch 491. Oscillating waveform output 475 is coupled to a negative input of comparator 477. An output of comparator 465 is coupled to a first input of AND gate 487. A leading edge blanking delay circuit 485 is coupled between the output of



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NAND gate 493 and a second input of AND gate 487. In one embodiment, there is a gate driver or a buffer between the output of the NAND gate 493 and the gate of the MOSFET (not shown). An output of AND gate 487 is coupled to a first input of OR gate 489. A second input of OR gate 489 is coupled to an output of comparator 477. An output of OR gate 489 is coupled to a reset input of latch 491. An output of latch 491 is coupled to a second input of AND gate 493. The output of AND gate 493 generates switching waveform 335.

Operation of power supply controller 139 of FIG. 4 is as follows. Beginning with negative current sensor 301, the gate of transistor 407 is fixed at  $V_{BG} + V_{TN}$  in one embodiment to approximately 2.3 volts. As a result, transistor 407 sets the voltage at multi-function terminal 149 to  $V_{BG}$  in one embodiment, which is approximately 1.25 volts, when current is pulled out of multi-function terminal 149. This current may be referred to as negative current since the current is being pulled out of power supply controller 139. In one embodiment, transistor 407 is sized such that it operates with a current density resulting in a voltage drop between the gate and source that is close to  $V_{TN}$ , wherein the  $V_{TN}$  is the threshold of the N channel transistor 407, when negative current flows from multi-function terminal 149.

When an external resistor (not shown) is coupled from multi-function terminal 149 to ground, the negative current flowing through the external resistor will therefore be  $V_{BG}$  divided by the value of the external resistor in accordance with Ohm's law. This negative current flowing out from multi-function terminal 149 passes through transistors 403 and is mirrored on to transistor 405. Current source 401 limits the negative current sourced by multi-function terminal 149. Therefore, even if multi-function terminal 149 is short-circuited to ground, the current is limited to a current less than the current supplied by current source 401. This current is less than the current source 401 by an amount that flows through the transistor 405. In one embodiment, the negative current that can be drawn from the multi-function terminal is limited to 200 microamps by the current source 401. In one embodiment, if more negative current than current source 401 is able to supply is pulled from multi-function terminal 149, the voltage at multi-function terminal 149 collapses to approximately 0 volts.

The current that flows through transistor 403 is mirrored to transistor 405. The current that flows through transistors 405 and 411 is the same since they are coupled in series. Since transistors 411 and 413 form a current mirror, the current flowing through transistor 413 is proportional to the negative current flowing through multi-function terminal 149. The current flowing through transistor 413 is compared to the current provided by current source 409. If the current through transistor 413 is greater than the current supplied by current source 409, the signal at the drain of transistor 413 will go low, which in one embodiment enables the power supply. Indeed, on/off signal 311 is received at an inverted input of NOR gate 445. Thus, when on/off signal 311 is low, the power supply is enabled. Therefore, by having a negative current greater than a particular threshold value, the power supply of the present invention is enabled in one embodiment. In one embodiment, the magnitude of that particular threshold value is approximately 50 microamps.

As mentioned above, the current flowing through transistor 411 is proportional to the negative current flowing out from multi-function terminal 149. As illustrated, transistor 419 also forms a current mirror with transistor 411. Therefore, the current flowing through transistor 419 is proportional to the current flowing through transistor 411.

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The current flowing through transistor 421 is the difference between the current supplied by current source 415 and the current flowing through transistor 419. For example, assume that the current supplied by current source 415 is equal to A. Assume further that the current flowing through transistor 419 is equal to B. In this case, the current flowing through transistor 421 is equal to A-B.

As illustrated, transistor 423 forms a current mirror with transistor 421. Therefore, the current flowing through transistor 423 is proportional to the current flowing through transistor 421. Continuing with the example above and assuming further that transistors 421 and 423 are equal in size, the current flowing through transistor 423 is also equal to A-B. Assuming further that current source 417 supplies a current equal to the current supplied by current source 415, which is assumed to be equal to A, then the current flowing through resistor 425 would be equal to A-(A-B), which is equal to B.

Therefore, the current flowing through resistor 425 is proportional to the current flowing through transistor 419, which is proportional to the current flowing through transistor 411, which is proportional to the negative current flowing out from multi-function terminal 149. Note that if the current flowing through transistor 419 is greater than the current supplied by current source 415, the current flowing through transistor 421 would be zero because the voltage at the drains of transistors 419 and 421 would collapse to approximately zero volts. This would result in the current flowing through transistor 423 to be zero. Thus, the current through resistor 425 cannot be greater than the current supplied by current source 417. However, as long as B is less than A, the current that flows through resistor 425 is equal to B. If B rises above A, the current that flows through resistor 425 is equal to A.

In one embodiment, resistor 425 is fabricated using the same or similar types of processes and diffusions or doped regions used in fabricating power MOSFET 495. As a result, the on resistance of resistor 425 follows or tracks the on resistance of power MOSFET 495 through varying operating conditions and processing variations.

The voltage across resistor 425 is reflected in external current limit adjuster signal 315, which is input to the negative input of comparator 465. In one embodiment, the negative input of comparator 465 is the threshold input of comparator 465. Therefore, the negative input of comparator 465 receives a voltage proportional to the negative current flowing out of multi-function terminal 149 multiplied by the resistance of resistor 425.

The positive input of comparator 465 is coupled to drain terminal 141 through resistor 461 of the voltage divider formed by resistor 461 and resistor 463. Therefore, the positive input of comparator 465 senses a voltage proportional to the drain current of power MOSFET 495 multiplied by the on resistance of power MOSFET 495.

When the voltage at the positive terminal of comparator 465 rises above the voltage provided by external current limit adjuster signal 315 to the negative terminal of comparator 465, the output of comparator 465 is configured to reset latch 491 through AND gate 487 and OR gate 489. By resetting latch 491, the on portion of a cycle of waveform 335 received at the gate of power MOSFET 495 is masked or cut short, which results in turning off power MOSFET 495 when the amount of current flowing through power switch 147 rises above the threshold.

In one embodiment, AND gate 487 also receives input from leading edge blanking delay circuitry 485. In one



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embodiment, leading edge blanking delay circuitry 485, using known techniques, temporarily disables current limit detection at the start, or during the leading edge portion, of an on transition of power MOSFET 495.

As shown in the embodiment illustrated in FIG. 4, latch 491 is set at the beginning of each cycle by switching waveform output 473. One way that latch 491 is reset, thereby turning off power MOSFET 495, is through the output of comparator 465. Another way to reset latch 491 is through the output of comparator 477, which will be discussed below in connection with maximum duty cycle adjuster 325.

With regard to positive current sensor 305, the gate of transistor 429 is coupled to the band gap voltage  $V_{BG}$ . In one embodiment, transistor 429 is sized such that it operates with a current density resulting in a drop between the source and gate close to  $V_{TP}$ , which is threshold of the P channel transistor 429, when positive current flows into multi-function terminal 149. In one embodiment, current that flows into multi-function terminal 149 is referred to as positive current since the current is being fed into the power supply controller 139. As a result, the voltage at multi-function terminal 149 is fixed at approximately  $V_{BG} + V_{TP}$  when positive current flows into multi-function terminal 149.

The gate voltages on the transistors 407 and 429 chosen in the embodiment discussed above are such that only one of transistors 407 and 429 are switched on at a time depending on the polarity of the current at the multi-function terminal. Stated differently, if transistor 407 is on, transistor 429 is off. If transistor 429 is on, transistor 407 is off. As result, if negative current sensor 301 is on, positive current sensor 305 is isolated from multi-function terminal 149. If positive current sensor 305 is on, negative current sensor 301 is isolated from multi-function terminal 149. Therefore, if there is negative current flowing through multi-function terminal 149, positive current sensor 305 is disabled. If there is positive current flowing through multi-function terminal 149, negative current sensor 301 is disabled.

In one embodiment, the positive current that flows into transistor 429 flows through transistor 431 since they are coupled in series. The positive current through multi-function terminal 149 flows into and is limited by current source 435. In one embodiment, if the positive current through multi-function terminal 149 is greater than an amount that current source 435 can sink minus the current in transistor 433, then the voltage at multi-function terminal 149 will rise and is clamped either by the circuitry driving the current or by the standard clamping circuitry that is used for protection purposes on external terminals such as the multi-function terminal, of a power supply controller. As shown, transistors 431 and 433 form a current mirror. Therefore, the current flowing through transistor 433 is proportional to the positive current that flows through transistor 431. The current that flows through the transistor 433 flows to transistor 427 since they are coupled in series. As shown, the gate of transistor 427 is coupled to the drain of transistor 427, which generates positive current sense signal 307.

Transistors 427 and 437 form a current mirror since the gate and drain of transistor 427 are coupled to the gate of transistor 437. Therefore, the current flowing through transistor 437 is proportional to the current flowing through transistor 427, which is proportional to the positive current. Current source 439 provides a reference current, which is compared to the current that flows through transistor 437. If

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the current flowing through transistor 437 rises above the current provided by current source 439, then the voltage at the drain of transistor 437, which is the under-voltage signal 319, goes high. When under-voltage signal 319 goes high and the output of NOR gate 445 will go low, indicating that there is no under-voltage condition.

Transistors 427 and 441 also form a current mirror since the gate and drain of transistor 427 are coupled to the gate of transistor 441. Therefore, the current flowing through transistor 441 is proportional to the current flowing through the transistor 427, which is proportional to the positive current. Current source 443 provides a reference current, which is compared to current that flows through transistor 441. As long as the current flowing through transistor 441 stays below the current provided by current source 443, then the voltage at the drain of transistor 441, which is the over-voltage signal 323, remains low. When over-voltage signal 323 remains low, the output of NOR gate 447 remains high assuming that there was no under-voltage condition indicated by under-voltage signal 319 and no remote off condition indicated by on/off signal 311.

The output of NOR gate 447 is enable/disable signal 331. In one embodiment, enable/disable signal 331 is high if on/off signal 311 is low, or under-voltage signal 319 is high and over-voltage signal 323 is low. Otherwise, enable/disable signal 331 is low.

In one embodiment, the oscillator 467 receives enable/disable signal 331 at the start/stop input 469. In one embodiment, oscillator 467 generates oscillating waveforms at oscillating waveform outputs 471, 473 and 475 while enable/disable signal 331 is high or active. In one embodiment, oscillator 467 does not generate the oscillating waveforms at oscillating waveform outputs 471, 473 and 475 while enable/disable signal 331 is low or in-active. In one embodiment, oscillator 467 begins generating oscillating waveforms starting with new complete cycles on a rising edge of enable/disable signal 331. In one embodiment, oscillator 467 completes existing cycles of the oscillating waveforms generated at oscillating waveform outputs 471, 473 and 475 before stopping the waveforms in response to a falling edge of enable/disable signal 331. That is, oscillator 467 stops generating the waveforms at a point just before the start of an on time of power switch of the next cycle in response to a falling edge of enable/disable signal 331.

In one embodiment, control terminal 145 supplies power to the circuitry of power supply controller 139 and also provides feedback to modulate the duty cycle of switching waveform 335. In one embodiment, control terminal 145 is coupled to the output of the power supply 101 through a feedback circuit to regulate the output voltage of the power supply 101. In one embodiment, an increase in the output voltage of power supply 101 results in the reduction in the duty cycle of switching waveform 335 through feedback received through control terminal 145. Therefore, if the regulation level of the output parameter of power supply 101 that is being controlled, such as output voltage or current or power, is exceeded during operation, additional feedback current is received through control terminal 145. This feedback current flows through resistor 455 and through a shunt regulator formed by transistor 457 and comparator 459. If no feedback current or control terminal current in excess of supply current is received through control terminal 145, the current through transistor 457 is zero. If the current through transistor 457 is zero, and assuming for the time being that there is no current through the diode 451, the current through resistor 479 is zero. If there is no current flowing through resistor 479, then the voltage drop across resistor 479 is zero.

If there is no voltage drop across resistor 479, there is no voltage drop across capacitor 483. As a result, the output of comparator 477 will remain low. If the output of comparator 477 remains low, and assuming for the time being that the output of AND gate 487 remains low, the output of latch 491 will remain high. In this case, the maximum duty cycle signal, which is produced by oscillator waveform output 471, will be generated at the output of AND gate 493. Thus, switching waveform 335 will have the maximum duty cycle produced by oscillator waveform output 471.

Therefore, when the voltage drop across resistor 479 remains at zero, the maximum duty cycle produced at oscillator waveform output 471 is not limited, assuming that the output of AND gate 487 remains low. This is because latch 491 is not reset through the output of comparator 477. However, when the feedback current or control terminal current in excess to the supply current is received through control terminal 145, this feedback current flows through transistor 457. As the amount of current flowing through the transistor 457 increases, the voltage drop across resistor 479 increases correspondingly. As a voltage drop across resistor 479 increases, the voltage drop across capacitor 483 will increase. In any given cycle, when the voltage on the oscillating waveform output 475 crosses below the voltage across the capacitor 483 the output of the comparator will go high and terminate the on-time of the switching waveform 335 or turn off the power switch 495. As a result, the duty cycle (on time as a fraction of the cycle time) of the switching waveform 335 decreases with increase in voltage drop across resistor 479.

In one embodiment, the oscillating waveform at oscillating waveform output 475 is a sawtooth waveform having a duty cycle and period equal to the maximum duty cycle waveform generated at oscillating waveform output 471. As the voltage drop across resistor 479 increases, the output of comparator 477 will go high closer to the beginning of each cycle. When the output of comparator 477 goes high, latch 491 will be reset through NOR gate 489. When latch 491 is reset, the on time of the of switching waveform: 335 is terminated for that particular cycle and switching waveform 335 remains low for the remainder of that particular cycle. Latch 491 will not be set again until the beginning of the next cycle through switching waveform output 473, assuming that there is a high or active enable/disable signal 331.

Referring now to maximum duty cycle adjuster signal 325, transistor 449 includes a source coupled to control terminal 145 and a gate coupled to the gate and drain of transistor 427 to receive positive current sense signal 307. Transistor 449 and transistor 427 also form a current mirror. Therefore, the current flowing through transistor 449 is proportional to the current flowing through transistor 427, which is proportional to the positive current flowing into multi-function terminal 149. The current that flows through diode 451 is the difference between the current that flows through transistor 449 and the current that flows into current source 453. The current that flows through current source 453 is set such that current will not begin to flow through diode 451 until the current flowing through transistor 449 rises above a threshold. In one embodiment, the above threshold value is chosen such that the maximum duty cycle is not reduced until the positive current flowing into multi-function terminal 149 rises above the threshold used for under-voltage comparison. In one embodiment, the threshold positive current used for under-voltage comparison is approximately 50 microamps and the threshold positive current used for maximum duty cycle adjustment is approximately 60 microamps.

When current begins to flows through diode 451, that current will be combined with current that flows through transistor 457. In one embodiment, the current that flows through diode 451 is maximum duty cycle adjustment signal 327. The current flowing through transistor 457 and diode 451 will flow through resistor 479. As discussed in detail above, current that flows through resistor 479 will result in the voltage drop across resistor 479, which results in a reduction in the maximum duty cycle of switching waveform 335. As the current that flows through resistor 479 increases, the maximum duty cycle of switching waveform 335 will be decreased.

FIG. 5 is a diagram illustrating some of the currents, voltages and duty cycles associated with the power supply controller 139 in accordance with teachings of the present invention. In particular, diagram 501 illustrates when the power supply is enabled in relation to the input current of multi-function terminal 149. The x-axis represents the positive or negative current flowing into or out of multi-function terminal 149. As illustrated, as positive input current rises from zero and crosses over 50 microamps, power supply controller 139 in one embodiment is enabled. At this time, an under-voltage condition is removed. If the current is above 50 microamps but then falls below zero microamps, power supply controller 139 is disabled. At this time, an under-voltage condition is detected. The difference between 50 microamps and zero microamps provides hysteresis, which provides for more stable operation during noise or ripple conditions in the input current.

As the input current rises above 225 microamps, the power supply is disabled. At this time, an over-voltage condition is detected. When the input current falls back below 215 microamps, the power supply is re-enabled. At this time, the over-voltage condition is removed. The difference between 225 microamps and 215 microamps provides hysteresis, which provides for more stable operation during noise or ripple conditions in the input current.

Continuing with diagram 501, when the negative current that flows out from multi-function terminal 149 rises in magnitude to a level above 50 microamps, which is illustrated as -50 microamps in FIG. 5, the power supply is enabled. At this time, the on/off feature of the present invention turns on the power supply. When the negative current falls in magnitude to a level below 40 microamps, which is illustrated as -40 microamps in FIG. 5, the power supply is disabled. At this time, the on/off feature of the present invention turns off the power supply. The difference between -50 microamps and 40 microamps provides hysteresis, which provides for more stable operation, during noise or ripple conditions in the input current.

It is worthwhile to note that in one embodiment the positive input current is clamped at 300 microamps and that the negative input current is clamped at 200 microamps. The positive input current would be clamped at 300 microamps when, for example, the multi-function terminal 149 is short-circuited to a supply voltage. The negative input current would be clamped at 200 microamps when, for example, the multi-function terminal is short-circuited to ground.

In diagram 503, the current limit through power switch 147 as adjusted by the present invention is illustrated. Note that the hysteresis of the under-voltage and over-voltage conditions are illustrated from zero microamps to 50 microamps and from 215 microamps to 225 microamps, respectively. In one embodiment, when positive input current is provided into multi-function terminal 149 and there is neither an under-voltage condition nor an over-voltage

1 with the U.S. International Trade Commission ("ITC") in an effort to obtain expedited relief to  
2 prevent continued infringement through importation of the infringing products into the United  
3 States. The District Court case was stayed pending the proceedings in the ITC. The ITC instituted  
4 an investigation, and a hearing was held before an Administrative Law Judge ("ALJ"), who found  
5 all asserted claims of the '908 patent to be valid and infringed and recommended an exclusion order  
6 against the infringing SG products. On August 11, 2006, the ITC issued an exclusion order against  
7 the infringing SG chips. SG appealed the ITC decision, but the Federal Circuit affirmed the ITC's  
8 findings in all respects.

9       25. After the findings that SG infringed the '908 patent and that the '908 patent was  
10 valid in the ITC trial and the issuance of the exclusion order, Fairchild purchased SG. Prior to its  
11 purchase of SG, Fairchild was itself also found to have infringed certain other of Power Integrations  
12 patents in a proceeding in the U.S. District Court for the District of Delaware. Like the ITC and the  
13 Federal Circuit, the Delaware Jury and Court both rejected Fairchild's challenges to the validity of  
14 these other Power Integrations patents as well.

15       26. Since the acquisition of SG, SG has operated as a wholly-owned subsidiary of  
16 Fairchild, and Defendants have continued to sell SG chips and to introduce new chips based on the  
17 SG architecture.

18       27. During the parties' prior litigation, SG initiated multiple challenges to the validity of  
19 the '908 patent via filing two separate requests for *ex parte* reexamination before the USPTO,  
20 raising a number of allegations of invalidity. On April 14, 2009, the USPTO issued Reexamination  
21 Certificate No. 6,538,908 C1, confirming the patentability of claims 1-10 and 19-34 of the '908. A  
22 true and correct copy of the '908 Reexamination Certificate is attached hereto as Exhibit D.

23       28. After the USPTO confirmed the validity of claims in all of the patents previously  
24 asserted against SG, Power Integrations contacted Defendants regarding their continued  
25 infringement in a letter dated August 10, 2009. Despite the USPTO's confirmation of the validity  
26 of the '908 patent and Power Integrations' prior success in proving infringement and validity in the  
27 ITC proceeding and on appeal, Defendants have refused to agree to stop infringing Power  
28 Integrations' patents.

condition, the current limit through power switch 147 is 3 amps. However, when negative current flows out from multi-function terminal 149, and the magnitude of the negative current rises above 50 microamps, which is illustrated as -50 microamps in FIG. 5, the current limit through power switch 149 is approximately 1 amp. As the magnitude of the negative current rises to 150 microamps, which is illustrated as -150 microamps in FIG. 5, the current limit through power switch 149 rises proportionally with the negative current to 3 amps. After the magnitude of the negative current rises above 150 microamps, the current limit of the power switch 149 remains fixed at 3 amps. Note that there is also the on/off hysteresis between -50 microamps and -40 microamps in diagram 503.

Diagram 505 illustrates the maximum duty cycle setting of power supply controller 139 in relation to the input current. Note that the hysteresis from -50 microamps to 40 microamps, from zero microamps to 50 microamps and from 215 microamps to 225 microamps as discussed above is included. In the embodiment illustrated in diagram 505, the maximum duty cycle is fixed at 75 percent until a positive input current of 60 microamps is reached. As the input current continues to increase, the maximum duty cycle continues to decrease until an input current of 225 microamps is reached, at which time the maximum duty cycle has been reduced to 33 percent. As illustrated, between 60 microamps and 225 microamps, the maximum duty cycle is inversely proportional to the positive input current. Note that when negative current flows through multi-function terminal 149, and when the power supply is enabled, the maximum duty cycle in one embodiment is fixed at 75 percent.

Diagram 507 illustrates the voltage at multi-function terminal, which is labeled in diagram 507 as line sense voltage, in relation to the input current. When negative current is flowing from multi-function terminal 149, the voltage at multi-function terminal 149 is fixed at the band gap voltage  $V_{BG}$ , which in one embodiment is 1.25 volts. When positive current is flowing into multi-function terminal 149, the voltage at multi-function terminal is fixed at the band gap voltage  $V_{BG}$  plus a threshold voltage  $V_{TP}$ , which in one embodiment sum to 2.3 volts. In the event that a negative current having a magnitude of more than 200 microamps is attempted to be drawn out of the multi-function terminal 149, the voltage at multi-function terminal 149 drops to approximately zero volts. In the event that a positive current of more than 300 microamps flows into multi-function terminal 149, the voltage at multi-function terminal 149 rises. In this case, the voltage will be limited by either by a standard clamp used at the multi-function terminal for the purpose of protection or by the external circuitry driving the multi-function terminal, whichever is lower in voltage.

It is appreciated that the currents, voltages, duty cycle settings and hysteresis settings described in connection with the present invention are given for explanation purposes only and that other values may be selected in accordance with teachings of the present invention. For example, in other embodiments, non hysteretic thresholds may be utilized. Thus the hysteresis values may be greater than or equal to zero.

FIG. 6A is timing diagram illustrating one embodiment of some of the waveforms of a power supply controller in accordance with teachings of the present invention. Referring to both FIGS. 4 and 6A, oscillating waveform output 475 of oscillator 467 generates a sawtooth waveform, which is received by comparator 477. Oscillating waveform output 471 of oscillator 467 generates a maximum duty cycle

signal, which is received by AND gate 493. Enable/disable signal 331, which is received at enable/disable input 469 of oscillator 467, is also illustrated. In FIG. 6A, the enable/disable signal 331 is active. Therefore, the sawtooth waveform of oscillating waveform output 475 and the maximum duty cycle waveform of oscillating waveform output 471 are generated. Note that the sawtooth waveform and the maximum duty cycle waveform have the same frequency and period. One cycle of each of these waveform occurs between time 601 and time 605. The peak of the sawtooth waveform occurs at the same time as the rising edge of the maximum duty cycle waveform. This aspect is illustrated at time 601 and at time 605. The lowest point of the sawtooth waveform occurs at the same time as the falling edge of the maximum duty cycle waveform. This aspect is illustrated at time 603.

Referring now to FIG. 6B, a timing diagram illustrating another embodiment of the waveforms of a power supply controller in accordance with teachings of the present invention is shown. From time 607 to time 609, the enable/disable signal 331 is low or inactive. In one embodiment, a low enable/disable signal 331 disables the power supply. A high or active enable/disable signal 331 enables the power supply. At time 609, the rising edge of enable/disable signal 331 occurs. At this time, oscillating waveform outputs 475 and 471 begin generating the sawtooth waveform and maximum duty cycle waveform, respectively. Note that a new complete cycle of each of these waveforms is generated in response to the rising edge of enable/disable signal 331 at time 609.

From time 609 to time 611, enable/disable signal 331 remains high or active. Thus, during this time, the sawtooth waveform and maximum duty cycle waveform are continuously generated.

At time 611, a falling edge of enable/disable signal 331 occurs. Before oscillator 467 discontinues generating the sawtooth waveform and the maximum duty cycle waveform, the existing cycles of each of these waveforms are allowed to complete. Stated differently, generation of the sawtooth waveform and the maximum duty cycle waveform is discontinued at a point just before the start of the on-time of the switching waveform 335 or the on-time of the power switch of the next cycle. This point in time is illustrated in FIG. 6B at time 613. Note that after time 613, the sawtooth waveform remains inactive at a high value and the maximum duty cycle waveform remains inactive at a low value.

At time 615, another rising edge of enable/disable signal 331 occurs. Therefore, the sawtooth waveform and the maximum duty cycle waveform are generated beginning at a new complete cycle of each waveform. As illustrated in FIG. 6B, a falling edge of enable/disable signal 331 occurs at time 617, which is immediately after the rising edge. However, the sawtooth waveform and maximum duty cycle waveforms are allowed to complete their then existing cycles. This occurs at time 619. After time 619, the waveforms remains inactive as shown during the time between time 619 and time 621, which is when another rising edge of enable/disable signal 331 occurs. At time 621, another new complete cycle of the sawtooth waveform and the maximum duty cycle waveform are generated. Since enable/disable signal 331 is deactivated at time 623, which occurs during a cycle of the sawtooth waveform and the maximum duty cycle waveform, these waveforms are deactivated after fully completing their respective cycles. Thus, by pulsing the on/off control signal at the multi-function terminal it is possible to synchronize the oscillator to the on/off pulse frequency.

FIG. 7 is a schematic of another embodiment of a power supply controller 139 in accordance with the teachings of the

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present invention. The power supply controller schematic shown in FIG. 7 is similar to the power supply controller schematic discussed above in FIG. 4. The primary difference between the power supply controller of FIGS. 4 and 7 is that oscillator 467 of FIG. 7 does not have an enable/disable input 469 coupled to receive enable/disable signal 331. As shown in the embodiment depicted in FIG. 7, the enable/disable signal 331 is used to directly gate the switching waveform at the input of AND gate 493. In this embodiment, the oscillator 467 is running all the time and switching waveform 335 will be gated on and off at any point in the cycle in response to the enable/disable signal 331.

To illustrate, FIG. 8 shows one embodiment of timing diagrams of switching waveforms of the power supply controller illustrated in FIG. 7. Referring to both FIGS. 7 and 8, oscillating waveform output 475 of oscillator 467 generates a sawtooth waveform, which is received by comparator 477. Oscillating waveform output 471 of oscillator 467 generates a maximum duty cycle signal, which is received by AND gate 493. Enable/disable signal 331, which is received by AND gate 493, and the output of AND gate 493, which is switching waveform 335, are also illustrated. In FIG. 8, the enable/disable signal 331 is active only some of the time. Therefore, the switching waveform 335 is switching only during those portions of time that the enable/disable signal 331 is active. When the enable/disable signal 331 is not active, switching waveform 335 does not switch.

In the foregoing detailed description, the method and apparatus of the present invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the present invention. The present specification and figures are accordingly to be regarded as illustrative rather than restrictive.

What is claimed is:

1. A power supply controller, comprising:
  - a power switch having first, second and third terminals, the first terminal to be coupled to a transformer of a power supply and the second terminal to be coupled to an input of the power supply;
  - a control circuit coupled to a control terminal of the power supply controller and the third terminal of the power switch, the control terminal coupled to an output of the power supply, the control circuit to generate a switching waveform to control the power switch; and
  - multi-function circuitry coupled between a multi-function terminal of the power supply controller and the control circuit, the switching waveform generated in response to the control terminal and the multi-function terminal.
2. The power supply controller of claim 1, wherein the multi-function circuitry comprises:
  - a negative current sensor coupled to the multi-function terminal, the negative current sensor to generate a negative current sense signal in response to the multi-function terminal if a voltage at the multi-function terminal is less than a first voltage, the negative current sensor isolated from the multi-function terminal if the voltage at the multi-function terminal is greater than the first voltage;
  - a positive current sensor coupled to the multi-function terminal, the positive current sensor to generate a positive current sense signal in response to the multi-function terminal if the voltage at the multi-function terminal is greater than a second voltage, the positive current sensor isolated from the multi-function terminal

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if the voltage at the multi-function terminal is less than the second voltage, wherein the second voltage is greater than the first voltage, the switching waveform generated in response to the negative current sense signal and the positive current sense signal.

3. The power supply controller of claim 1 wherein the multi-function circuitry comprises on/off circuitry coupled to the control circuit and responsive to the multi-function terminal, the on/off circuitry to control the control circuit to start and to stop the switching waveform in response to the multi-function terminal.

4. The power supply controller of claim 1 wherein the multi-function circuitry comprises external current limit adjuster circuitry coupled to the control circuit and responsive to the multi-function terminal, the external current limit adjuster circuitry to control the control circuit to adjust a current limit of the power switch in response to the multi-function terminal.

5. The power supply controller of claim 1 wherein the multi-function circuitry comprises over-voltage comparator circuitry coupled to the control circuit and responsive to the multi-function terminal, the over-voltage comparator circuitry to control the control circuit to start and to stop the switching waveform in response to the multi-function terminal.

6. The power supply controller of claim 1 wherein the multi-function circuitry comprises maximum duty cycle adjuster circuitry coupled to the control circuit and responsive to the multi-function terminal, the maximum duty cycle adjuster circuitry to adjust the maximum duty cycle of the switching waveform in response to the multi-function terminal.

7. The power supply controller of claim 1, wherein a voltage at the multi-function terminal is substantially equal to a first constant voltage if there is a negative current flowing through the multi-function terminal.

8. The power supply controller of claim 1, wherein a voltage at the multi-function terminal is substantially equal to a second constant voltage if there is a positive current flowing through the multi-function terminal.

9. The power supply controller of claim 1 wherein the first, second and third terminals of the power switch are drain, source and gate terminals, respectively.

10. The power supply controller of claim 1 wherein the first terminal is to be coupled to a primary winding of the transformer.

11. A method for controlling a power supply, comprising: generating a switching waveform to control a power switch of a power supply controller coupled to a primary winding of the power supply;

adjusting the switching waveform in response to a control terminal of the power supply controller coupled to an output of the power supply; and

adjusting the switching waveform in response to a signal at a multi-function terminal of the power supply controller.

12. The method of claim 11 wherein adjusting the switching waveform in response to the signal at the multi-function terminal comprises generating a negative current sense signal if a current flowing through the multi-function terminal flows out of the power supply controller from the multi-function terminal.

13. The method of claim 11 further comprising adjusting a current limit of the power switch in response to the signal at the multi-function terminal.

14. The method of claim 11 wherein adjusting the switching waveform in response to the signal at the multi-function

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terminal comprises enabling and disabling the switching waveform in response to the signal at the multi-function terminal.

15. The method of claim 11 wherein adjusting the switching waveform in response to the signal at the multi-function terminal comprises generating a positive current sense signal if a current flowing through the multi-function terminal flows into the power supply controller through the multi-function terminal.

16. The method of claim 11 further wherein adjusting the switching waveform in response to the signal at the multi-function terminal comprises adjusting a maximum duty cycle of the switching waveform in response to the signal at the multi-function terminal.

17. The method of claim 11 further comprising identifying an under-voltage in the power supply in response to the signal at the multi-function terminal.

18. The method of claim 11 further comprising identifying an over-voltage in the power supply in response to the signal at the multi-function terminal.

19. A power supply controller, comprising:

a power switch coupled between a transformer of a power supply and an input terminal of the power supply;

a control circuit coupled to the power switch and a control terminal of the power supply controller, the control terminal coupled to an output of the power supply, the control circuit to generate a switching waveform to control the power switch; and

multi-function circuitry providing a plurality of functions coupled between a multi-function terminal of the power supply controller and the control circuit, the control circuit adapted to generate the switching waveform generated in response to the control terminal and the multi-function circuitry.

20. The power supply controller of claim 19 wherein the plurality of functions provided by the multi-function circuitry include at least two or more of current limit adjustment, under-voltage detection, over-voltage detection, maximum duty cycle adjustment and on/off control circuitry at the same time in the power supply controller.

21. The power supply controller of claim 20 wherein the current limit adjustment, under-voltage detection, over-voltage detection, maximum duty cycle adjustment and on/off control circuitry are adapted to be responsive to a signal at the multi-functional terminal.

22. The power supply controller of claim 20 wherein at least a portion of the plurality of functions provided by the multi-function circuitry are adapted to be implemented during startup operation of the power supply.

23. The power supply controller of claim 20 wherein at least a portion of the plurality of functions provided by the multi-function circuitry are adapted to be implemented during normal operation of the power supply.

24. The power supply controller of claim 20 wherein at least a portion of the plurality of functions provided by the multi-function circuitry are adapted to be implemented during fault conditions in of the power supply.

25. The power supply controller of claim 20 wherein at least a portion of the plurality of functions provided by the multi-function circuitry are adapted to be implemented during standby operation of the power supply.

26. A power supply controller circuit, comprising:

a multi-function circuit coupled to receive a signal at a multi-function terminal for adjusting a current limit of

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a power switch, the multi-function circuit to generate a current limit adjustment signal in response to the signal; and

a control circuit coupled to receive the current limit adjustment signal, the control circuit coupled to adjust the current limit of a current through the power switch in response to the current limit adjustment signal.

27. The power supply controller circuit of claim 26 wherein the control circuit is further coupled to an output of a power supply through a control terminal of the power supply controller circuit, the control circuit adapted to control a switching of the power switch in response to the output of the power supply.

28. The power supply controller circuit of claim 26 wherein the control circuit includes a control terminal adapted to provide a supply voltage for the power supply controller.

29. The power supply controller circuit of claim 28 wherein an optocoupler is coupled to an output of a power supply, wherein an output transistor of the optocoupler is coupled between the control terminal and the multi-function terminal such that the current limit of the current through the power switch is adjusted in a closed loop to regulate the output of the power supply.

30. A method for controlling a power supply, comprising: sensing a signal at a multi-function terminal of a power supply controller;

controlling a current flowing through a primary winding of the power supply with a power switch coupled to the primary winding; and

adjusting a current limit of the current flowing through the primary winding in response to the signal at the multi-function terminal.

31. The method of claim 30 further comprising:

receiving a feedback signal from an output of the power supply at a control terminal; and

regulating the output of the power supply in response to the feedback signal and the current limit of the current flowing through the primary winding.

32. The method of claim 30 wherein adjusting the current limit of the current flowing through the primary winding comprises increasing the current limit of the current flowing through the primary winding in response to sensing an increase in the signal at the multi-function terminal of a power supply controller.

33. The method of claim 30 wherein adjusting the current limit of the current flowing through the primary winding comprises decreasing the current limit of the current flowing through the primary winding in response to sensing a decrease in the signal at the multi-function terminal of a power supply controller.

34. The method of claim 30 wherein controlling the current flowing through the primary winding of the power supply comprises:

switching the power switch in response to a switching waveform; and

adjusting the switching waveform in response to the signal at the multi-function terminal of a power supply controller.

\* \* \* \* \*





US006538908C1

(12) **EX PARTE REEXAMINATION CERTIFICATE (6767th)**  
**United States Patent**  
**Balakrishnan et al.**

(10) **Number:** **US 6,538,908 C1**  
(45) **Certificate Issued:** **Apr. 14, 2009**

(54) **METHOD AND APPARATUS PROVIDING A MULTI-FUNCTION TERMINAL FOR A POWER SUPPLY CONTROLLER**

**FOREIGN PATENT DOCUMENTS**

JP 11215820 8/1999

**OTHER PUBLICATIONS**

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(US); **Leif O. Lund**, San Jose, CA (US)

(73) **Assignee:** **Power Intergrations, Inc.**, Sunnyvale, CA (US)

**Reexamination Request:**

No. 90/007,790, Oct. 25, 2005

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Patent No.: **6,538,908**

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Appl. No.: **10/167,557**

Filed: **Jun. 11, 2002**

**Related U.S. Application Data**

(63) Continuation of application No. 09/405,209, filed on Sep. 24, 1999, now Pat. No. 6,462,971.

(51) **Int. Cl.**  
**H02M 3/24** (2006.01)  
**H02M 1/00** (2006.01)  
**H02M 3/335** (2006.01)

(52) **U.S. Cl.** ..... **363/95; 363/16; 323/299**

(58) **Field of Classification Search** ..... None  
See application file for complete search history.

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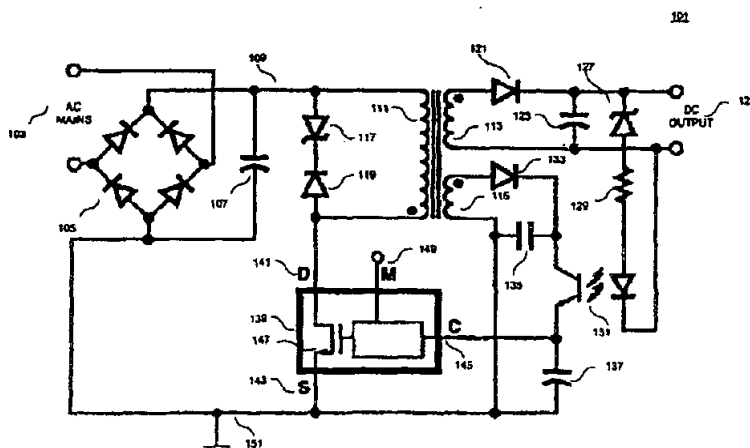
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*Primary Examiner*—My-Trang Ton

(57) **ABSTRACT**

A power supply controller having a multi-function terminal. In one embodiment, a power supply controller for switched mode power supply includes a drain terminal, a source terminal, a control terminal and a multi-function terminal. The multi-function terminal may be configured in a plurality of ways providing any one or some of a plurality of functions including on/off control, external current limit adjustments, under-voltage detection, over-voltage detection and maximum duty cycle adjustment. The operation of the multi-function terminal varies depending on whether a positive or negative current flows through the multi-function terminal. A short-circuit to ground from the multi-function terminal enables the power supply controller. A short-circuit to a supply voltage from the multi-function terminal disables the power supply controller. The current limit of an internal power switch of the power supply controller may be adjusted by externally setting a negative current from the multi-function terminal. The multi-function terminal may also be coupled to the input DC line voltage of the power supply through a resistance to detect an under-voltage condition, an over-voltage condition and/or adjust the maximum duty cycle of power supply controller. Synchronization of the oscillator of the power supply controller may also be realized by switching the multi-function terminal to power or ground at the desired times.





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US 6,538,908 C1

**1**  
**EX PARTE**  
**REEXAMINATION CERTIFICATE**  
**ISSUED UNDER 35 U.S.C. 307**

THE PATENT IS HEREBY AMENDED AS  
INDICATED BELOW.

**2**  
AS A RESULT OF REEXAMINATION, IT HAS BEEN  
DETERMINED THAT:

5 The patentability of claims 1-10 and 19-34 is confirmed.  
Claims 12-18 are cancelled.

\* \* \* \* \*





US006212079B1

(12) **United States Patent**  
**Balakrishnan et al.**

(10) **Patent No.:** **US 6,212,079 B1**  
(45) **Date of Patent:** **Apr. 3, 2001**

(54) **METHOD AND APPARATUS FOR  
IMPROVING EFFICIENCY IN A SWITCHING  
REGULATOR AT LIGHT LOADS**

5,747,977 \* 5/1998 Hwang ..... 323/284  
5,912,552 \* 6/1999 Tateishi ..... 323/285

\* cited by examiner

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*Primary Examiner*—Adolf Deneke Bethane

(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor &  
Zafman, LLP

(73) **Assignee:** **Power Integrations, Inc.**, Sunnyvale,  
CA (US)

(57) **ABSTRACT**

(\*) **Notice:** Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 0 days.

A switching regulator that operates at a frequency for a first range of feedback signal values and at a variable frequency without skipping cycles for a second range of feedback signal values. In one embodiment, a switching regulator for a switched mode power supply includes a power switch coupled between drain and source terminals of the switching regulator, which are to be coupled to control the delivery of power to an output of a power supply. A control terminal of the switching regulator is to be coupled to an output of the power supply. The switching regulator includes a control circuit coupled to the control terminal and generates a feedback signal that is responsive to the output of the power supply. The control circuit also generates a drive signal that is coupled to control the switching of the power switch. The control circuit generates the drive signal responsive to the feedback signal. The drive signal has a fixed frequency for a first range of feedback signal values and at a variable frequency without skipping cycles for a second range of feedback signal values.

(21) **Appl. No.:** **09/608,161**

(22) **Filed:** **Jun. 30, 2000**

(51) **Int. Cl.<sup>7</sup>** ..... **H02M 3/335; G05F 1/56**

(52) **U.S. Cl.** ..... **363/21; 363/97; 323/284**

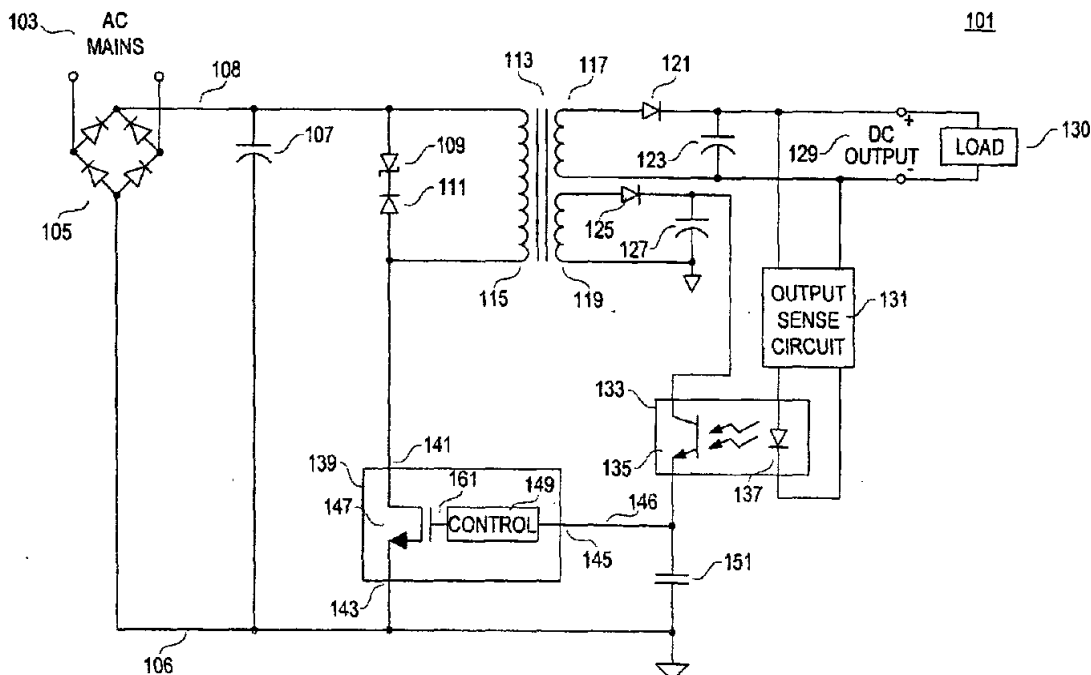
(58) **Field of Search** ..... **363/20, 21, 97,  
363/131; 323/282, 283, 284, 285**

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4,849,869 \* 7/1989 Tanuma et al. .... 363/21  
5,430,633 \* 7/1995 Smith ..... 363/20

**29 Claims, 4 Drawing Sheets**



29. Defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '908 patent in this District and elsewhere by making, using, selling, offering to sell devices, and/or importing devices, including power supply controller integrated circuit devices, covered by one or more claims of the '908 patent, and/or contributing to or inducing the same by third-parties, all to the injury of Power Integrations. In particular, Defendants' power supply controller products that include what Defendants characterize as providing "Constant Output Power Limit" functionality by sensing line voltage variations through sensing current at an input pin of the controller (for example, the "V<sub>IN</sub> pin"), and further providing additional functions from that same pin, infringe Power Integrations' '908 patent.

**30. Defendants' acts of infringement have injured and damaged Power Integrations.**

31. Defendants' acts of infringement have been, and continue to be, willful so as to warrant the enhancement of damages awarded as a result of their infringement. In particular, despite Power Integrations' prior notice of infringement as early as 2004, despite the prior determinations of infringement and validity by the ITC and the subsequent affirmance of those determinations by the Court of Appeals for the Federal Circuit, despite the '908 patent emerging from reexamination, and despite Power Integrations' renewed notice to Defendants of their infringement, Defendants have failed to commit to ceasing all infringement of the '908 patent.

32. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until Defendants are enjoined from further infringement/ this Court.

### THIRD CAUSE OF ACTION

**INFRINGEMENT OF U.S. PATENT NO. 6,212,079**

33. The allegations of paragraphs 1-10 are incorporated for this Third Cause <sup>on as</sup> though fully set forth herein.

34. Power Integrations is now, and has been since its issuance, the assignee and owner of all right, title, and interest in United States Patent No. 6,212,079, entitled "Apparatus for Improving Efficiency in a Switching Regulator at Light Loads" ("tent"),

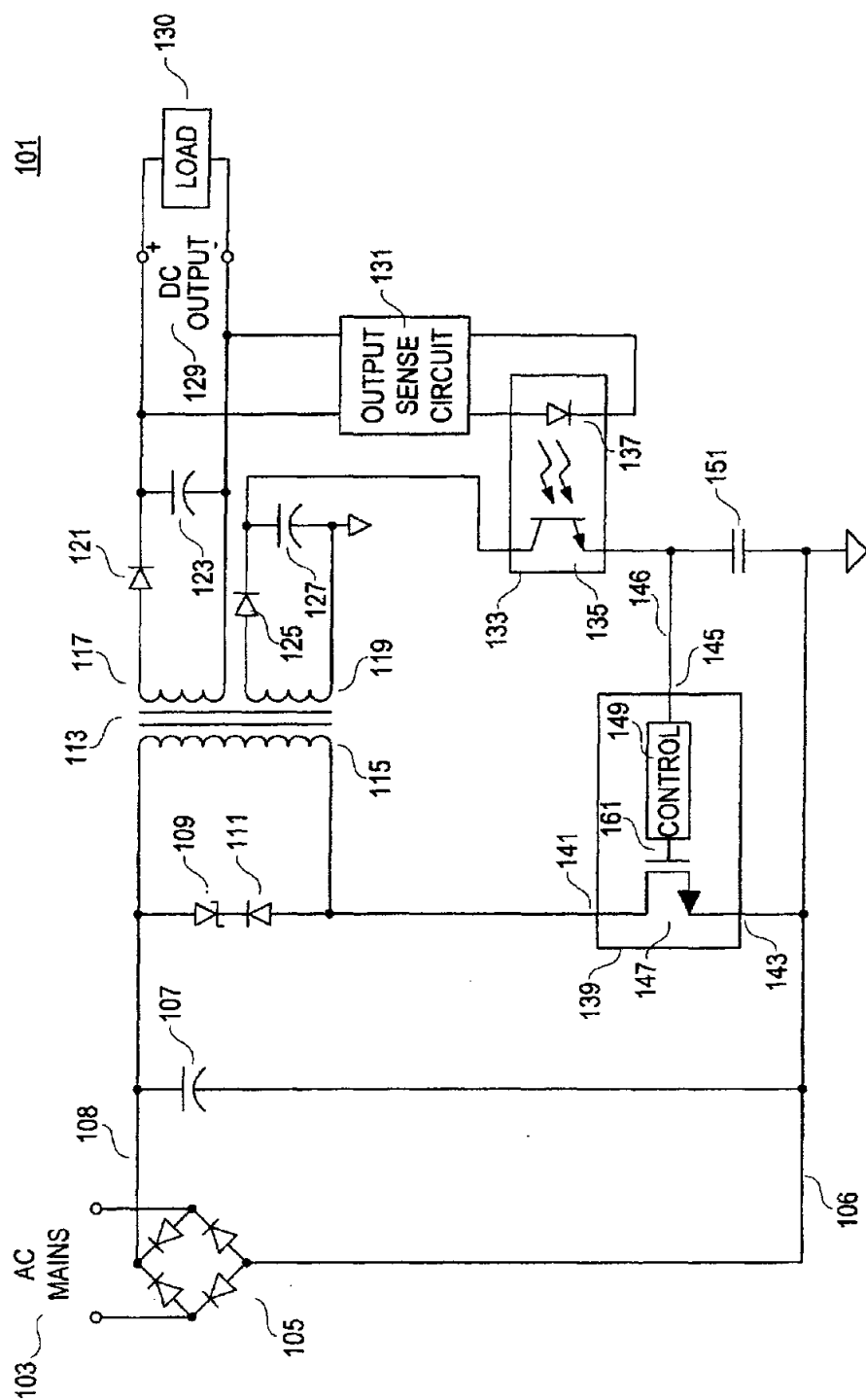
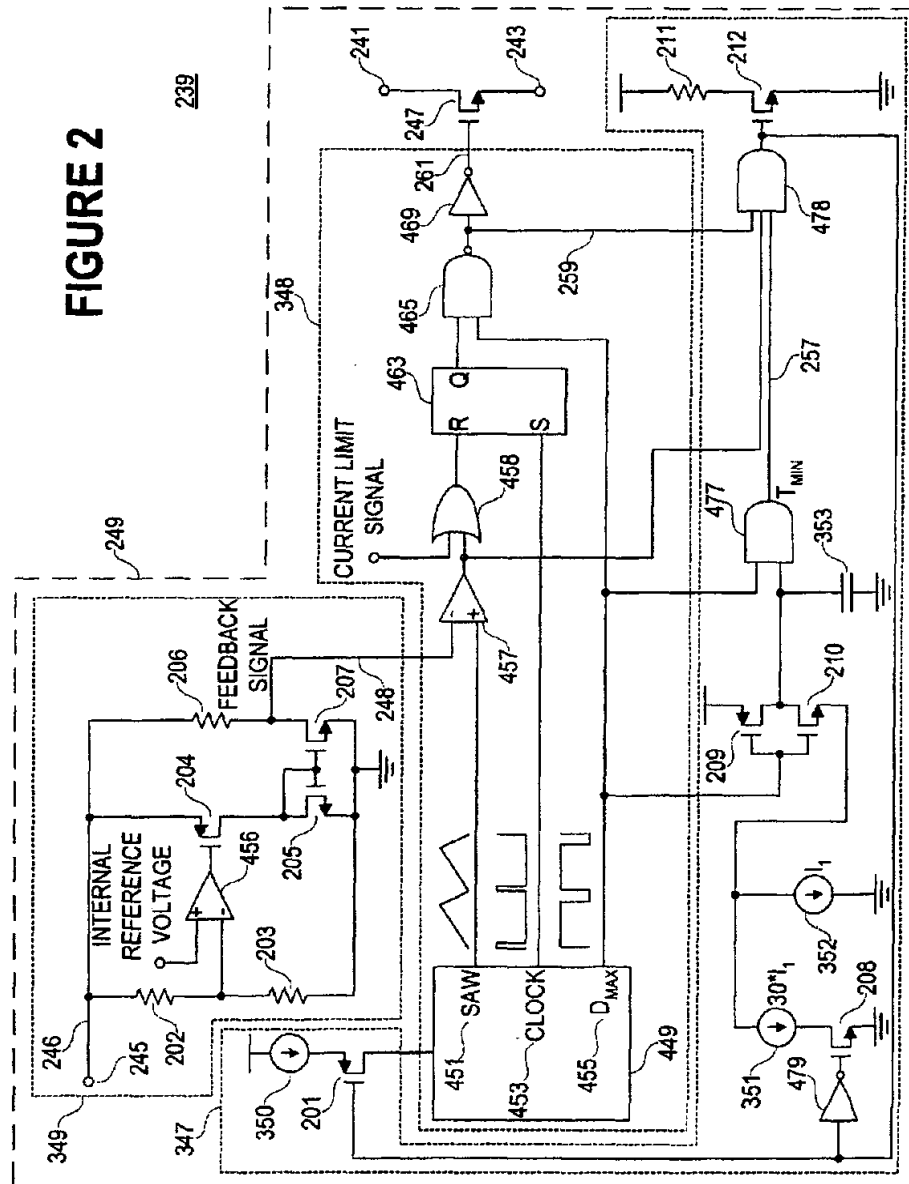


FIGURE 1

FIGURE 2





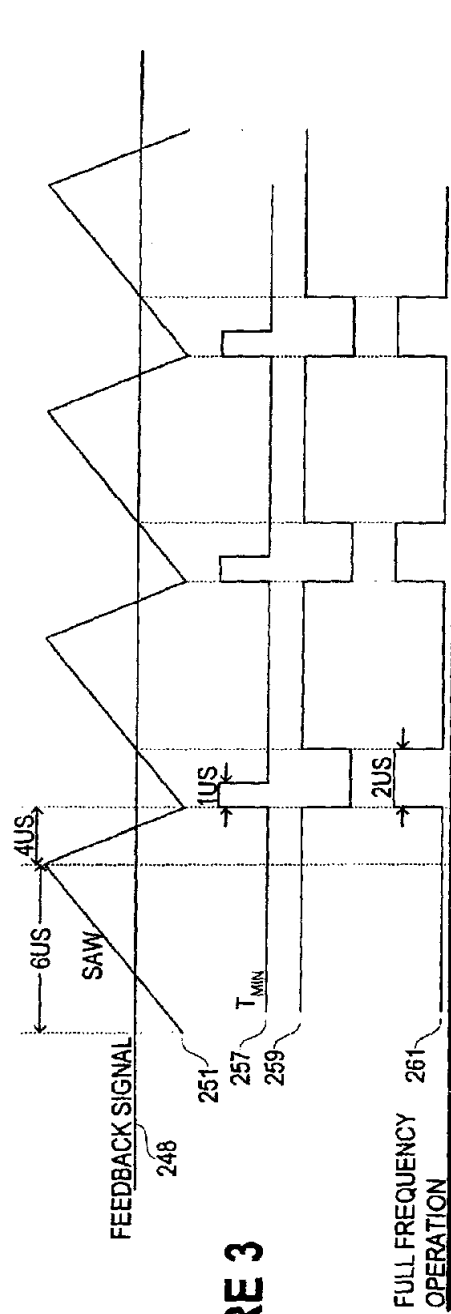


FIGURE 3

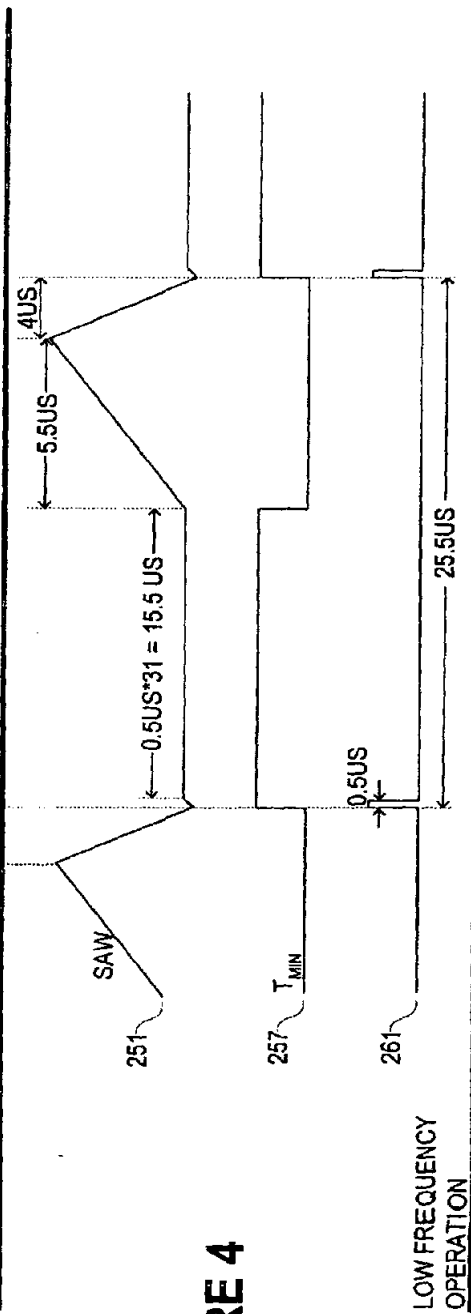


FIGURE 4

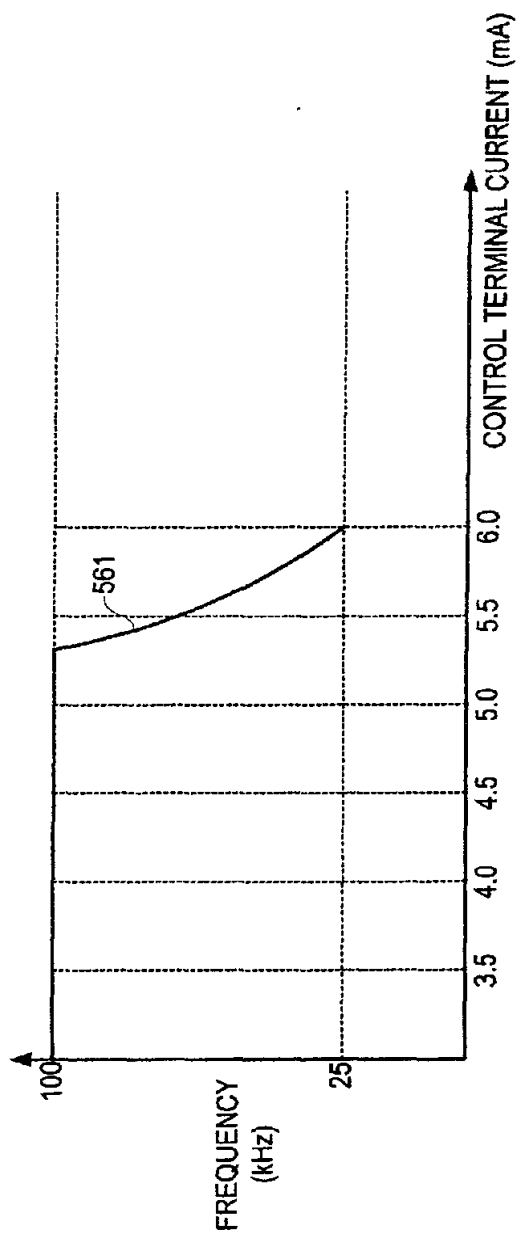


FIGURE 5

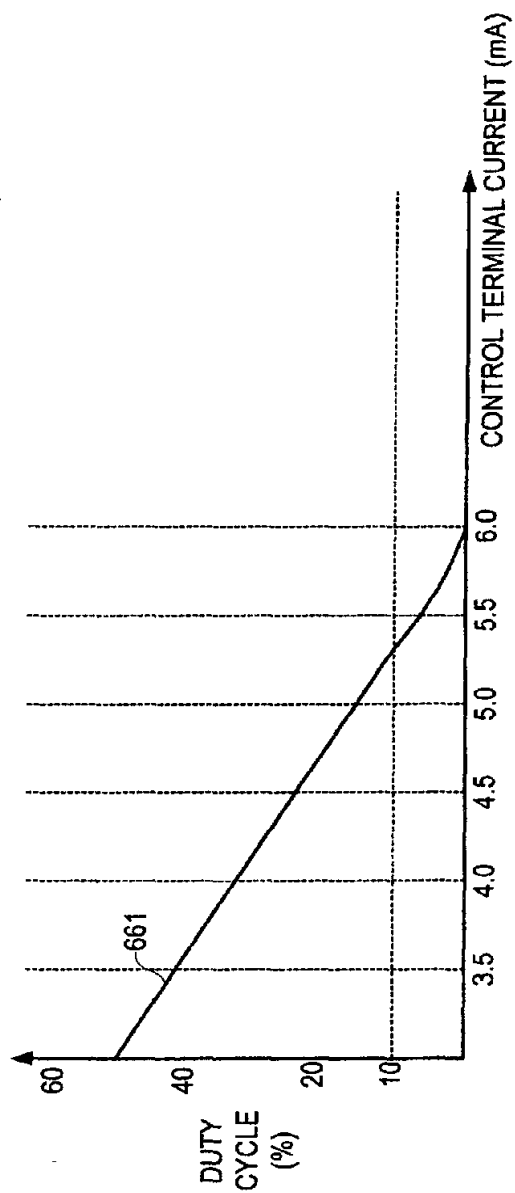


FIGURE 6

1

## METHOD AND APPARATUS FOR IMPROVING EFFICIENCY IN A SWITCHING REGULATOR AT LIGHT LOADS

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates generally to power supplies and, more specifically, the present invention relates to a switching regulator.

#### 2. Background Information

Electronic devices use power to operate. Switched mode power supplies are commonly used due to their high efficiency and good output regulation to power many of today's electronic devices. In a known switched mode power supply, a low frequency (e.g. 50 or 60 Hz mains frequency), high voltage alternating current (AC) is converted to high frequency (e.g. 30 to 300 kHz) AC, using a switched mode power supply control circuit. This high frequency, high voltage AC is applied to a transformer to transform the voltage, usually to a lower voltage, and to provide safety isolation. The output of the transformer is rectified to provide a regulated DC output, which may be used to power an electronic device. The switched mode power supply control circuit usually provides output regulation by sensing the output and controlling it in a closed loop.

A switched mode power supply may include an integrated circuit switching regulator, which may include an output transistor coupled in series with a primary winding of the transformer. Energy is transferred to a secondary winding of the transformer by turning on and off of the output transistor in a manner controlled by the switching regulator to provide a clean and steady source of power at the DC output. The transformer of a switched mode power supply may also include another winding called a bias or feedback winding. In some switched mode power supplies, the feedback or control signal can come through an opto-coupler from a sense circuit coupled to the DC output. The feedback control signal may be used to modulate a duty cycle of a switching waveform generated by the switching regulator. The duty cycle is defined as the ratio of the on time to the switching period of the output transistor. If there is a large load at the DC output of the power supply, the switching regulator responds to this situation by increasing the duty cycle and thereby delivering more power to the load. If the load becomes lighter, then the switching regulator senses this change through the feedback signal and reduces the duty cycle.

If the load is further reduced and if the power delivered to the DC output cannot be reduced indefinitely, then the DC output voltage increases, resulting in poor output regulation. This unfavorable situation becomes worse if the load is completely removed. To improve the output regulation, a constant load may be connected internal to the power supply. However, because the internal load is always connected, even when there is no load at the DC output, the power supply efficiency is decreased. The power supply efficiency loss is generally due to three components: (1) DC operating power that keeps the switching regulator circuitry operating, (2) the switching losses that are due to switching of the switching regulator output transistor and its drivers—switching losses are directly proportional to the operating frequency, and (3) the power that is consumed by the internal load.

In order to improve efficiency, a switching regulator may use a method called cycle skipping. Cycle skipping method involves reducing the duty cycle as the load decreases, and

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when the duty cycle is reduced down to a predetermined minimum duty cycle, it alternatively switches for some duration of time and stays idle for another duration of time depending on the load. During this mode, if the load increases very slightly, the output transistor will switch at minimum duty cycle for a short time until the power demanded by the load is delivered and then stop switching again. In theory, the cycle skipping mode decreases the switching losses at light loads since switching occurs as intermittent groups of pulses. Also, cycle skipping eliminates the need for the constant internal load. However, if the groups of pulses occur at a frequency that is within the audio range and the minimum duty cycle is larger than optimum, then the power supply may create an undesirable audio noise. In addition, cycle skipping degrades the output ripple since it typically occurs in groups of pulses and therefore the energy is delivered to the load intermittently.

### SUMMARY OF THE INVENTION

Switching regulator methods and apparatuses are disclosed. In one embodiment, a switching regulator includes a power switch coupled between first and second terminals. The first terminal is to be coupled to an energy transfer element of a power supply and the second terminal is to be coupled to a supply rail of the power supply. A control circuit is coupled to a third terminal and the power switch. The third terminal is to be coupled to an output of the power supply. The control circuit is coupled to generate a feedback signal responsive to the output of the power supply. The control circuit is coupled to switch the power switch in response to the feedback signal. The control circuit is coupled to switch the power switch at a fixed switching frequency for a first range of feedback signal values and coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values. Additional features and benefits of the present invention will become apparent from the detailed description, figures and claims set forth below.

### BRIEF DESCRIPTION OF THE DRAWINGS

The present invention detailed illustrated by way of example and not limitation in the accompanying figures.

FIG. 1 is a schematic illustrating one embodiment of a power supply including a switching regulator in accordance with the teachings of the present invention.

FIG. 2 is a schematic illustrating one embodiment of a switching regulator in accordance with the teachings of the present invention.

FIG. 3 is a timing diagram illustrating waveforms of one embodiment of switching regulator operating at full frequency in accordance with the teachings of the present invention.

FIG. 4 is a timing diagram illustrating waveforms of one embodiment of switching regulator operating at a lower frequency in accordance with the teachings of the present invention.

FIG. 5 is a diagram illustrating one embodiment of a relationship between frequency and current in one embodiment of switching regulator in accordance with the teachings of the present invention.

FIG. 6 is a diagram illustrating one embodiment of a relationship between duty cycle and current in one embodiment of switching regulator in accordance with the teachings of the present invention.

### DETAILED DESCRIPTION

Method and an apparatus for regulating a power supply are disclosed. In the following description, numerous spe-

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cific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific detail need not be employed to practice the present invention. In other instances, well-known materials or methods have not been described in detail in order to avoid obscuring the present invention.

The present invention improves the efficiency of a power supply switching regulator with pulse width modulation by decreasing the operating frequency at light loads. Switching losses are decreased with one embodiment of the present invention since switching losses are directly proportional to operating frequency. Audio noise problems associated with present day switching regulators are no longer a problem because the minimum operating frequency of a switching regulator in accordance with the teachings of the present invention is chosen to be above audible frequency. One embodiment of the present invention also improves output ripple since the pulse width modulation is continuous in nature and not intermittent.

To illustrate, FIG. 1 is a block diagram showing a power supply 101 including one embodiment of a switching regulator 139 in accordance with the teachings of the present invention. As shown, a bridge rectifier 105 and capacitor 107 are coupled to rectify and filter an input alternating current (AC) voltage received at AC mains 103. In one embodiment, a positive power supply rail 108 and a ground power supply rail 106 are provided across capacitor 107. The rectified voltage generated by bridge rectifier 105 and capacitor 107 is received at a primary winding 115 of an energy transfer element, such as transformer 113. In one embodiment, transformer 113 includes a secondary winding 117 and a bias winding 119. Diode 121 and capacitor 123 rectify and filter DC output 129, whereas diode 125 and capacitor 127 rectify and filter the bias winding.

The switching regulator 139 includes a drain terminal 141 coupled to the primary winding 115 and a source terminal 143 coupled to the ground rail 106. In one embodiment, switching regulator 139 includes a control circuit 149, which generates a drive signal 161 to switch a power switch 147 to transfer the energy to the secondary winding 117 using transformer 113. Diode 111 and Zener 109 are used for clamping the drain terminal 141.

A load 130 is configured to be coupled across output 129. A feedback loop is formed from output 129 through output sense circuit 131 to a control terminal 145 of the switching regulator 139. The feedback loop includes the output sense circuit 131 and opto-coupler 133. The opto-coupler 133 includes a transistor 135 that is optically coupled to a photodiode 137. An output sense signal 146 responsive to output sense circuit 131 is coupled to be received by control terminal 145 of the switching regulator 139. Output sense signal 146 may be a current or a voltage. The combined bias supply current as well as the feedback current is provided to the control terminal 145 by the opto-coupler 133 using the bias winding 119. Thus, the control terminal 145 may be characterized as a supply voltage ( $V_s$ )/feedback terminal for switching regulator 139. This control terminal 145 is therefore frequently referred to as a combined electrical terminal. An external capacitor 151 is connected between control terminal 145 and ground.

FIG. 2 is a schematic illustrating one embodiment of a switching regulator 239 in accordance with the teachings of the present invention. In one embodiment, switching regulator 239 of FIG. 2 may be utilized in place of switching regulator 139 of FIG. 1. As shown, an example embodiment

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of switching regulator 239 includes a power switch 247 coupled between a drain terminal 241 and a source terminal 243. A gate of power switch 247 is coupled to be switched in response to a drive signal 261 generated by control circuit 249.

Control circuit 249 includes a feedback signal circuit 349 coupled to generate a feedback signal 248 responsive to an output sense signal 246 coupled to be received by control terminal 245. In one embodiment, an internal bias current for switching regulator 239 during normal operation is provided by an internal shunt regulator coupled to control terminal 245. In one embodiment, an external capacitor, such as capacitor 151 of FIG. 1, is coupled to control terminal 245. For instance, one embodiment of switching regulator 239 is powered after an initial turn-on by current into control terminal 245 through opto-coupler 133 from output sense circuit 131, which is coupled to the output 129 of power supply 101, as shown in FIG. 1. Part of the current that goes into control terminal 245 powers up the circuitry of switching regulator 239 and the remainder is shunted to ground by the shunt regulator. Feedback signal 248 is extracted from the amount of current that is shunted to ground. If there is a substantial load 130 coupled to the output 129 of power supply 101, then all available current goes to the load.

To illustrate, attention is directed to feedback signal circuit 349 of FIG. 2. As shown, comparator 456 includes a positive terminal coupled to an internal reference voltage. The negative terminal of comparator 456 is connected to a voltage that is a fraction of the control terminal 245 voltage through a voltage divider network of resistors including resistors 202 and 203. Comparator 456 compares the internal reference voltage to the fraction of control terminal 245 voltage. If the internal reference voltage is lower than the fraction of control terminal 245 voltage, indicating that the control terminal 245 voltage is at the nominal voltage, the output of comparator 456 goes low, turning on transistor 204. Any excess current that is going into the control terminal 245 is shunted to ground through transistors 204 and 205. Since the transistors 205 and 207 form a current mirror, a proportional fraction of this shunt current is used as the feedback current in transistor 207. The feedback current is converted to a feedback voltage signal through resistor 206, from which feedback signal 248 is generated.

An example embodiment of control circuit 249 includes a pulse width modulator (PWM) circuit 348. PWM circuit 348 generates drive signal 261 in response to feedback signal 248, which is used to control the duty cycle of power switch 247. PWM circuit 348 includes an oscillator 449 that generates three signals: SAW 451, CLOCK 453 and DMAX 455. As illustrated, the DMAX 455 signal is high during the ramp-up of SAW 451 and DMAX 455 is low during the ramp-down of SAW 451. In one embodiment, the CLOCK 453 signal is a short pulse generated at the low to high transition of DMAX 455. The CLOCK 453 signal is coupled to the S input of flip-flop 463 to set flip-flop 463.

When the CLOCK 453 signal goes high, the Q signal output of the flip-flop 463 goes high and remains high until the flip-flop 463 is reset by the R input of flip-flop 463 going high at a later time. The Q signal output of flip-flop 463 is coupled to one of the inputs of the NAND gate 465. The other input of the NAND gate 465 comes from the DMAX 455 signal of the oscillator 449. Since DMAX 455 is also high during this time, the output of NAND gate 465 is low and the output of the inverter 469 is high. In one embodiment, the output of inverter 469 is drive signal 261 coupled to switch power switch 247.

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When drive signal 261 is high, the power switch 247 is on. In one embodiment, drive signal 261 is coupled to turn off power switch 247 when either of the following conditions are met: the reset R input of the flip-flop 463 goes high, or, DMAX 455 of oscillator 449 goes low, which corresponds to maximum duty cycle condition during start-up or an overload condition. The reset R input of the flip-flop 463 goes high if the output of the comparator 457 goes high, or, if the current limit signal input of OR gate 458 goes high.

As shown, one input of OR gate 458 is coupled to receive the current limit signal and the other input of OR gate 458 is coupled to receive an output of comparator 457. In one embodiment, the current limit signal going high indicates that the current through the power switch 247 has exceeded a prescribed limit and the power switch 247 is immediately turned off. The output of comparator 457 goes high when the SAW 451 signal of oscillator 449 is higher than the feedback signal 248 coming from the drain of transistor 207. In one embodiment, the feedback signal 248 is a very slow moving signal—almost a DC level signal in comparison to the SAW 451 signal of oscillator 449. In one embodiment, the SAW 451 signal is a 100 kHz saw-tooth signal.

In one embodiment, PWM circuit 348 operates under at least three different conditions: (1) when the feedback signal 248 is less than the "valleys" of the SAW 451 signal, (2) when the feedback signal 248 is greater than the "peaks" of the SAW 451 signal, and (3) when the feedback signal 248 is in between the "peaks" and "valleys" of the SAW 451 signal.

When there is a considerable current through the resistor 206, there is a corresponding voltage drop across resistor 206 and feedback signal 248 is below the "valleys" of the SAW 451 signal. In one embodiment, a large amount of current through the resistor 206 indicates that there is large amount of current being dumped into the control terminal 246, which in turn indicates that the power demand by load 130, which is coupled to the output 129 of power supply 101, is low. In this situation, the positive terminal of the comparator 457 is always greater than the negative terminal and the output of the comparator 457 is always high, which keeps the R input of flip-flop 463 high through OR gate 458. When CLOCK 453 signal sets the flip-flop 463 through the S input, the Q output of flip-flop 463 is ready to go high and pull the gate of power switch 473 high to turn on power switch 473. However, since R input of the flip-flop 463 is kept high, the flip-flop 463 is reset immediately and the Q output of flip-flop 463 goes back down immediately, never allowing the power switch 247 to turn on.

In one embodiment, the feedback signal 248 is greater than the "peaks" of the SAW 451 signal when there is not enough current through the resistor 206 to drop the voltage of feedback signal 248 down. In one embodiment, this is the case when the output 129 is heavily loaded by load 130. In this situation, the positive terminal of the comparator 457 is always less than the negative terminal and the output of the comparator 457 is always low, keeping the R input of flip-flop 463 low and never resetting the flip-flop 463. This means that after the CLOCK 453 signal turns on the power switch 473 by setting the flip-flop 463, which makes the Q output of flip-flop 463 go high, the power switch 247 is not turned off until the DMAX 455 signal goes from high to low, or until the power switch 247 reaches current limit, allowing the output transistor to remain on for the maximum duty cycle or until power switch 247 reaches its current limit.

In one embodiment, when the feedback signal is less than the "peaks," but greater than the "valleys" of the SAW 451

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signal, the power supply 101 is operating within its nominal load range. In this case, PWM 348 will set the proper duty cycle for drive signal 261 in response to feedback signal 248 to keep the output 129 of power supply 101 regulated.

In one embodiment, control circuit 249 also includes a timer circuit 347 in accordance with the teachings of the present invention. In one embodiment, if the duty cycle of drive signal 261 is larger than 10%, the switching regulator 239 operates at a full frequency. In one embodiment, the full frequency is 100 kHz. It is appreciated of course that actual values provided in this disclosure, such as the 100 kHz frequency value, are provided for explanation purposes and that other actual values may be utilized in accordance with the teachings of the present invention. For purposes of this disclosure, the duty cycle of drive signal 261 is equal to the on-time of drive signal 261 divided by the period T of drive signal 261. The period T is equal to the on-time+off-time of drive signal 261. Thus, for a drive signal 261 with a full frequency of 100 kHz, the period T of each cycle of drive signal 261 is equal to  $\frac{1}{100}$  kHz or 10  $\mu$ s and the on-time of a 10% duty cycle signal is equal to 1  $\mu$ s. Thus, the off-time of a 10% duty cycle signal is equal to 10  $\mu$ s-1  $\mu$ s, or 9  $\mu$ s. It is appreciated that PWM circuit 348 adjusts the duty cycle of drive signal 261 in response feedback signal 248, which is responsive to the level of the load 130 coupled to output 129 as well as the input voltage of power supply 101.

In one embodiment, there are two modes of operation for a switching regulator 239 in accordance with the teachings of the present invention—full frequency and low frequency.

In one embodiment, the on-time of the power switch 247, which is responsive to feedback signal 248, determines whether switching regulator 239 operates at full frequency or low frequency. In one embodiment, when the on-time of drive signal 261 is greater than 1  $\mu$ s, the PWM circuit 348 operates in full frequency mode. When the on-time of drive signal 261 is less than 1  $\mu$ s, the PWM circuit 348 operates in low frequency mode. Therefore, since the duty cycle of drive signal 261 is responsive to feedback signal 248, the PWM circuit 348 operates in full frequency mode for one range of values for feedback signal 248 and PWM circuit 348 operates in low frequency mode for another range of values for feedback signal 248.

In one embodiment, switching regulator 239 is operated in full and low frequency modes as follows. A signal designated TMIN 257 is derived from the DMAX 455 signal. In one embodiment, TMIN 257 includes a pulse that is generated at each rising edge of DMAX 455. As illustrated, the duration of the pulse of TMIN 257 is determined by a capacitor 353 and current sources 351 and 352.

In one embodiment, capacitor 353 is coupled to be discharged through current sources 351 and 352 through transistor 210. In one embodiment, current source 351 draws charge at a rate 30 times greater than current source 352 from capacitor 353. When both current sources 351 and 352 are on at the same time to discharge capacitor 353, the duration of the TMIN 257 pulse width will be 1  $\mu$ s, 10% of the full frequency period of one embodiment of drive signal 261. In one embodiment, the current source 352 is always activated to discharge capacitor 353. However, the current source 351 is only activated to discharge capacitor 353 when the output of inverter 479 is high, or output of AND gate 478 is low. In one embodiment, AND gate 478 output will always be low if the gate of power switch 247 is on for longer than 1  $\mu$ s since AND gate 478 combines an inverted drive signal 261 (from the output of NAND gate 465) with TMIN 257. In one embodiment, when the drive signal 261 is on for longer than 1  $\mu$ s, the AND gate 478 output remains

low and transistor 201 remains on to keep oscillator 449 unaffected. In one embodiment, the frequency of drive signal 261 remains constant at 100 kHz in this case.

In one embodiment, as the duty cycle of drive signal 261 falls below 10% in response to feedback signal 248, the switching regulator 239 goes into low frequency operation. In one embodiment, as the duty cycle of drive signal 261 drops below 10%, or the on-time of drive signal 261 falls below 1  $\mu$ s, the output of the NAND gate 465 goes high while TMIN 257 is still high. During this time, if the status of drive signal 261 was determined through the feedback signal 248, instead of the current limit signal received at the input of OR gate 458, the output of the comparator 456 is also high. With all of the inputs of AND gate 478 being high, the output of AND gate 478 goes high and turns off transistor 201, cutting off the current into the oscillator 449 and suspending oscillations generated by oscillator 449.

In one embodiment, oscillator 449 maintains the value of SAW 451 at its last voltage magnitude, and the signals CLOCK 453 and DMAX 455 stop switching in response to oscillator 449 being suspended in response to transistor 201 being turned off. In one embodiment, when the output of AND gate 478 goes high, the output of inverter 479 goes low and transistor 208 turns off, which deactivates the current source 351 from discharging capacitor 353. Since the current that discharges the capacitor 353 is 31 times smaller now that current source 351 is deactivated, capacitor 353 discharges at a slower rate and remains charged for a longer amount of time. Consequently, the remaining on-time of TMIN 257 is increased by 31 times. As a result, the pulse width of TMIN 257 is increased from a fixed 1  $\mu$ s value to the value determined by the following equation:

$$\text{For DSPW} > 1 \mu\text{s: TMINPW} = 1 \mu\text{s};$$

$$\text{for DSPW} < 1 \mu\text{s: TMINPW} = ((1 \mu\text{s} - \text{DSPW}) * 31) + \text{DSPW} \quad (\text{Eq. 1})$$

where TMINPW is TMIN 257 pulse width and DSPW is drive signal 261 pulse width.

The oscillator 449 is suspended from switching for the duration of TMIN 257 pulse width minus the drive signal 261 pulse width and then released. When released, the operation of oscillator 449 resumes from where it left off and SAW 451 signal ramps up from the point at where it had been suspended. Accordingly, the switching period of drive signal 261 is increased from 10  $\mu$ s of full frequency operation to a value determined by the following equation:

$$\text{For DSPW} < 1 \mu\text{s: LFPDS} = (\text{TMINPW} - \text{DSPW}) + 10 \mu\text{s} \quad (\text{Eq. 2})$$

where LFPDS is low frequency period of drive signal 261 and TMINPW is TMIN 257 pulse width.

To illustrate, FIGS. 3 and 4 show full frequency and low frequency operation, respectively, of a switching regulator in accordance with the teachings of the present invention. In particular, FIG. 3 shows full frequency operation, which in one embodiment occurs when feedback signal 248 is in a range that causes the duty cycle of drive signal 261 to be greater than 10%. As shown in FIG. 3, feedback signal 248 is in between the "peaks" and "valleys" of SAW 251 signal. SAW 251 signal rises in from "valley" to "peak" in 6  $\mu$ s and falls from "peak" to "valley" in 4  $\mu$ s, which results in a full operating frequency of 100 kHz. In the example shown, drive signal has an on-time of 2  $\mu$ s or a duty cycle of 20%, which is greater than 10%. Accordingly, switching regulator 239 operates in full frequency mode. The inverted drive signal 259 keeps both current sources 351 and 352 activated all the time, allowing capacitor 353 to be discharged at the

faster rate for an entire 1  $\mu$ s. Thus, TMIN 257 has a pulse width or on-time of 1  $\mu$ s.

In comparison, FIG. 4 shows low frequency operation, which in one embodiment occurs when feedback signal 248 is in a range that causes the duty cycle of drive signal 261 to be less than 10%. In the particular example illustrated in FIG. 4, the on-time of drive signal 261 is only 0.5  $\mu$ s, which is less than 1  $\mu$ s. As shown, since the on-time of drive signal 261 is only 0.5  $\mu$ s, which is less than 1  $\mu$ s, capacitor 353 is still not fully discharged when current source 351 is deactivated and oscillator 449 is suspended. As shown, SAW 251 signal is caused to be held at the voltage when oscillator 449 was suspended and TMIN 257 now remains high for more than 1  $\mu$ s since capacitor 353 is discharged at a slower rate as a result of current source 351 being deactivated. Indeed, as shown, TMIN 257 remains high for the next 0.5  $\mu$ s \* 31 = 15.5  $\mu$ s. After TMIN 257 goes low, the operation of oscillator 449 is resumed and SAW 251 signal continues to oscillate from where it left off to rise to its "peak" in 5.5  $\mu$ s and subsequently fell to its "valley" in the normal 4  $\mu$ s.

In the illustrated example of FIG. 4, the switching frequency of drive signal 261 is reduced down to 39.2 kHz and the period of the drive signal has been increased to 25.5  $\mu$ s (0.5  $\mu$ s + 15.5  $\mu$ s + 5.5  $\mu$ s + 4  $\mu$ s). If the voltage of feedback signal 248 goes down more, the switching frequency of drive signal 261 decreases further in accordance with the teachings of the present invention. Note that the frequency of drive signal 261 is reduced without skipping cycles of drive signal 261 in accordance with the teachings of the present invention. Instead, the period of each cycle is increased to reduce the frequency of drive signal 261. In one embodiment, both the on-time and the off-time of each cycle of the drive signal 261 are adjusted simultaneously when increasing the period of the drive signal 261 in accordance with the teachings of the present invention.

In one embodiment, the lowest frequency that the power supply controller can go to can be calculated using the formulas above. In particular, assuming that the as the feedback signal 248 voltage decreases down to the voltage of the "valleys" of the SAW 251 signal, the on-time of drive signal 261 reduces to a substantially zero or negligible amount. In this case, using Equations 1 and 2 above:

$$\text{TMINPW} = ((1 \mu\text{s} - 0 \mu\text{s}) * 31) + 0 \mu\text{s} = 31 \mu\text{s}, \quad (\text{Eq. 3})$$

$$\text{LFPDS} = (\text{TMINPW} - 0 \mu\text{s}) + 10 \mu\text{s} = 41 \mu\text{s} \quad (\text{Eq. 4})$$

where TMINPW is TMIN 257 pulse width and LFPDS is low frequency period of drive signal 261. Thus, the period of drive signal 261 at the lowest frequency in this particular embodiment is 41  $\mu$ s.

The low frequency period of 41  $\mu$ s corresponds to a frequency of  $1/41 \mu\text{s}$ , or 24.4 kHz. Since the lowest switching frequency of 24.4 kHz is higher than the human audible frequency range of 20 to 20 kHz, a power supply 101 regulated with a switching regulator in accordance with the teachings of the present invention will not produce any audible noise, even at its lowest frequency.

Referring back to the embodiment shown in FIG. 2, timer circuit 347 also includes a transistor 212 switched in response to the output of AND gate 478. Transistor 212 acts as a switch to allow current to flow through resistor 211. The purpose of resistor 211 and transistor 212 is to keep the current consumption of switching regulator 239 during low frequency operation the same as the current consumption was during full frequency operation. As discussed earlier, one embodiment of switching regulator 239 is powered by a current into the control terminal 245 through opto-coupler

133 from output sense circuit coupled 131 to the output 129 of the power supply 101. In one embodiment, part of the current that goes into the control terminal 245 powers up the circuitry of switching regulator 239 and the remainder of the current is shunted to ground by the shunt regulator. The feedback signal 248 is extracted from the amount of the current that is shunted to ground.

As the frequency of drive signal 261 decreases during the low frequency operation, the power consumed due to switching of the internal circuitry of switching regulator 239 decreases, resulting in less current going into the circuitry of switching regulator 239 and more current being shunted to ground. As the current being shunted to ground increases, the portion of this current that is being used for extracting the feedback signal 248 would also increase, causing the feedback signal 248 to go lower. Correspondingly, the switching frequency of drive signal 261 would then go lower due to decreased current consumption of the switching regulator 239.

Thus, to keep the current consumption of the switching regulator substantially constant, additional current is drawn in low frequency mode operation through resistor 211 and transistor 212 to compensate for the difference in switching losses between full and low frequency operating modes of switching regulator 239 in accordance with the teachings of the present invention. If the additional current is greater than the reduction of power consumption, then, the pulse width modulation gain, i.e. the duty cycle versus control terminal 245 current, will be slightly reduced.

FIGS. 5 and 6 are diagrams illustrating the relationships of frequency vs. current 561, and duty cycle vs. current 661, respectively, in one embodiment of switching regulator in accordance with the teachings of the present invention. In particular, FIG. 6 shows that as the current into the control terminal 245 increases, the duty cycle of drive signal 261 decreases. In one embodiment, the duty cycle of drive signal 261 decreases in a linear type fashion relative to the current into control terminal 245 across the full and low frequency modes of the switching regulator in accordance with the teachings of the present invention.

FIG. 5 shows that in one embodiment as the duty cycle of drive signal 261 decreases, the switching frequency of drive signal 261 remains fixed until the duty cycle is reduced to a value such as 10%. As the duty cycle of drive signal 261 falls below 10%, in one embodiment, the frequency of drive signal 261 starts to decrease gradually, all the way down to approximately 25 kHz, by which time the duty cycle of drive signal 261 goes down to 0%. In one embodiment, the frequency of drive signal 261 decreases in a nearly linear type fashion in response to control terminal 245 current across the full and low frequency modes of the switching regulator in accordance with the teachings of the present invention.

In one embodiment, feedback signal 248 is responsive to the control terminal 245 current. Therefore, for one range of feedback signal 248 values, the switching regulator 239 operates at a fixed frequency and for another range of feedback signal 248 values, the frequency of operation of the switching regulator 239 is decreased in response to the feedback signal 248. In one embodiment, the boundary of fixed frequency operation and low frequency operation is a feedback signal 248 value that corresponds to a 10% duty cycle.

In one embodiment of the present invention, switching regulator 239 is operated at a full frequency operation at 130 kHz. In this embodiment, the on-time of drive signal 261 that corresponds to the boundary at which switching regu-

lator 239 is operated in either full frequency or low frequency can be adjusted by adjusting the TMIN 257 time constant when both current sources 351 and 352 are on. In one embodiment, the minimum frequency of drive signal 261 is 40 kHz. In another embodiment, switching regulator 239 is operated at a full frequency operation at 65 kHz with a minimum frequency for drive signal of 20 kHz.

In the foregoing detailed description, the method and apparatus of the present invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the present invention. The present specification and figures are accordingly to be regarded as illustrative rather than restrictive.

What is claimed is:

1. A switching regulator, comprising:

a power switch coupled between first and second terminals, the first terminal to be coupled to an energy transfer element of a power supply and the second terminal to be coupled to a supply rail of the power supply;

a control circuit coupled to a third terminal and the power switch, the third terminal to be coupled to an output of the power supply, the control circuit coupled to generate a feedback signal responsive to the output of the power supply, the control circuit coupled to switch the power switch in response to the feedback signal, the control circuit coupled to switch the power switch at a fixed switching frequency for a first range of feedback signal values, the control circuit coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values.

2. The switching regulator of claim 1 wherein the control circuit comprises:

a feedback signal circuit coupled to the third terminal, the feedback signal circuit coupled to generate the feedback signal; and

a pulse width modulator circuit coupled to switch the power switch in response to the feedback signal.

3. The switching regulator of claim 1 wherein the first and second ranges of the feedback signal correspond to first and second ranges of levels of a load coupled to the output of the power supply.

4. The switching regulator of claim 2 wherein the first and second ranges of the feedback signal correspond to first and second ranges of on-time values of a drive signal generated by the pulse width modulator circuit to switch the power switch.

5. The switching regulator of claim 2 wherein the first and second ranges of the feedback signal correspond to first and second ranges of duty cycle percentage values of a drive signal generated by the pulse width modulator circuit to switch the power switch.

6. The switching regulator of claim 2 wherein an off-time value of a drive signal generated by the pulse width modulator circuit to switch the power switch varies as a function of a level of a load coupled to the output of the power supply to vary the switching frequency of the power switch without skipping cycles for the second range of feedback signal values.

7. The switching regulator of claim 2 wherein on-time and off-time values of a drive signal generated by the pulse width modulator circuit to switch the power switch vary simultaneously as a function of a level of a load coupled to the output of the power supply to vary the switching frequency

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of the power switch without skipping cycles for the second range of feedback signal values.

8. The switching regulator of claim 7 wherein the off-time value of the drive signal is varied as a function of the on-time value and a first on-time value of the drive signal, the first on-time value of the drive signal corresponding to an on-time of the drive signal at a boundary between the first and second ranges of feedback signal values.

9. The switching regulator of claim 2 wherein the switching frequency of the power switch is reduced without skipping cycles for the second range of feedback signal values as a level of load coupled to the output of the power supply is reduced.

10. The switching regulator of claim 9 wherein the switching frequency of the power switch is reduced without skipping cycles to a minimum frequency when a duty cycle percentage value of a drive signal generated by the pulse width modulator circuit to switch the power switch is substantially equal to zero percent.

11. A power supply, comprising:

an energy transfer element having an energy transfer element input and an energy transfer element output coupled to an output of the power supply;

a switching regulator circuit including a power switch coupled to the energy transfer element input, and a control circuit coupled to the power switch and the output of the power supply, the control circuit coupled to generate a feedback signal responsive to the output of the power supply, the control circuit coupled to switch the power switch in response to the feedback signal, the control circuit coupled to switch the power switch at a fixed switching frequency for a first range of feedback signal values, the control circuit coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values.

12. The power supply of claim 11 wherein the control circuit comprises:

a feedback signal circuit coupled to the output of the power supply, the feedback signal circuit coupled to generate the feedback signal; and

a pulse width modulator circuit coupled to switch the power switch in response to the feedback signal.

13. The power supply of claim 12 further comprising an output sense circuit coupled between the output of the power supply and the switching regulator circuit, the output sense circuit coupled to provide an output sense signal to the switching regulator that is proportional to an output voltage or current supplied by the output of the power supply, wherein a duty cycle variation provided by a drive signal generated by the pulse width modulator circuit to switch the power switch is inversely proportional to the output sense signal.

14. The power supply of claim 11 wherein the first and second ranges of the feedback signal correspond to first and second ranges of levels of a load coupled to the output of the power supply.

15. The power supply of claim 12 wherein the first and second ranges of the feedback signal correspond to first and second ranges of on-time values of a drive signal generated by the pulse width modulator circuit to switch the power switch.

16. The power supply of claim 12 wherein the first and second ranges of the feedback signal correspond to first and second ranges of duty cycle percentage values of a drive signal generated by the pulse width modulator circuit to switch the power switch.

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17. A method for regulating a power supply, comprising: switching with a drive signal a power switch coupled to an energy transfer element of the power supply to control power delivered to an output of the power supply;

generating a feedback signal in response to the output of the power supply;

maintaining a frequency of the drive signal at a fixed frequency for a first range feedback signal values; and varying the frequency of the drive signal without skipping cycles in response to the feedback signal for a second range of feedback signal values.

18. The method for regulating the power supply of claim 17 further comprising varying a duty cycle of the drive signal substantially in response to the feedback signal.

19. The method for regulating the power supply of claim 17 wherein generating the feedback signal in response to the output of the power supply comprises monitoring a current representative of a level of the load coupled to the output of the power supply.

20. The method for regulating the power supply of claim 18 wherein generating the feedback signal in response to the output of the power supply comprises monitoring an on-time of the drive signal.

21. The method for regulating the power supply of claim 20 wherein monitoring the on-time of the drive signal comprises timing the on-time of the drive signal with a timer circuit, the method further comprising suspending operation temporarily of an oscillator circuit if the on-time of the drive signal is less than a first on-time value.

22. The method for regulating the power supply of claim 21 wherein timing the on-time of the drive signal with the timer circuit comprises

discharging a capacitor at a first rate during the on-time of the drive signal; and

discharging the capacitor at a second rate during an off-time of the drive signal, the first rate greater than the second rate.

23. The method for regulating the power supply of claim 22 further comprising maintaining a voltage level of a suspended oscillating signal generated by the oscillator circuit while the operation of the oscillator circuit is temporarily suspended.

24. The method for regulating the power supply of claim 23 further comprising resuming operation of the oscillator circuit after the capacitor has been discharged.

25. A switching regulator, comprising:

a power switch coupled between first and second terminals;

a control circuit coupled to a third terminal and coupled to the power switch, the control circuit coupled to receive an output sense signal responsive to an output of a power supply, the control circuit coupled to generate a drive signal to switch the power switch in response to the output sense signal to control the output of the power supply; and

a timer circuit included in the control circuit, the timer circuit coupled to time an on-time of the drive signal, the timer coupled to the control circuit to vary a switching frequency of the drive signal without skipping cycles if the on-time of the drive signal is less than a first on-time value, the drive signal to have a fixed switching frequency if the on-time of the drive signal is greater than the first on time value.

26. The switching regulator of claim 25 wherein the timer circuit comprises a capacitor that is coupled to be charged



1 which was duly and legally issued on April 3, 2001. A true and correct copy of the '079 patent is  
2 attached hereto as Exhibit E.

3 35. On June 28, 2004, Power Integrations filed a complaint for patent infringement  
4 against SG in this District because SG was infringing several Power Integrations patents, including  
5 the '079 patent. Thereafter, Power Integrations filed a similar complaint for patent infringement  
6 with the U.S. International Trade Commission ("ITC") in an effort to obtain expedited relief to  
7 prevent continued infringement through importation of the infringing products into the United  
8 States. The District Court case was stayed pending the proceedings in the ITC. Though Power  
9 Integrations had initially asserted the '079 patent in the ITC, it voluntarily narrowed its assertion of  
10 patents and claims in such a way that it proceeded to a hearing on the '398 and '908 patents, as  
11 discussed above. The ITC hearing was held before an Administrative Law Judge ("ALJ"), and the  
12 ALJ found all remaining asserted claims valid and infringed, and recommended an exclusion order  
13 against the infringing SG products. On August 11, 2006, the ITC issued an exclusion order against  
14 the infringing SG chips. SG appealed the ITC decision, but the Federal Circuit affirmed the ITC's  
15 findings in all respects. Thereafter, with the exclusion order in place, the parties voluntarily agreed  
16 to dismiss the District Court case, but their agreement explicitly recognized that Power Integrations  
17 could re-file the complaint again.

18 36. After the ITC trial and the issuance of the exclusion order, Fairchild purchased SG.  
19 Prior to its purchase of SG, Fairchild was itself also found to have infringed certain other of Power  
20 Integrations patents in a proceeding in the U.S. District Court for the District of Delaware. Like the  
21 ITC and the Federal Circuit, the Delaware Jury and Court both rejected Fairchild's challenges to the  
22 validity of these other Power Integrations patents as well.

23 37. Since the acquisition of SG, SG has operated as a wholly-owned subsidiary of  
24 Fairchild, and Defendants have continued to sell SG chips and to introduce new chips based on the  
25 SG architecture.

26 38. During the parties' prior litigation, SG initiated multiple challenges to the validity of  
27 the '079 patent via filing two separate requests for *ex parte* reexamination before the USPTO,  
28 raising a number of allegations of invalidity. On May 5, 2009, the USPTO issued Reexamination

13

and discharged in response to the drive signal, the capacitor to be discharged at a first rate during the on-time of the drive signal, the capacitor coupled to be discharged at a second rate during an off-time of the drive signal, the first rate greater than the second rate.

27. The switching regulator of claim 26 wherein the timer circuit further comprises first and second current sources coupled to discharge the capacitor at the first rate, the second current source coupled to discharge the capacitor at the second rate.

28. The switching regulator of claim 26 wherein the control circuit comprises an oscillator circuit coupled to

14

generate an oscillating signal, the oscillator circuit to suspend generating the oscillating signal if the on-time of the drive signal ends prior to the capacitor being discharged, the oscillator circuit coupled to resume generating the oscillating signal after the capacitor has been discharged.

29. The switching regulator of claim 28 wherein the oscillator circuit is coupled to maintain a voltage level of the oscillating signal while the oscillator circuit is suspended, the oscillator circuit is coupled to resume the oscillating signal from the maintained voltage level.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,212,079 B1  
DATED : April 3, 2001  
INVENTOR(S) : Balakrishnan et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

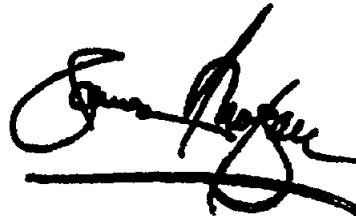
Title page.

*Primary Examiner*, replace examiner last name "Bethane" and insert -- Berhane --.

Signed and Sealed this

Twenty-second Day of January, 2002

Attest:

A handwritten signature in black ink, appearing to read "James E. Rogan", written over a horizontal line.

Attesting Officer

JAMES E. ROGAN  
*Director of the United States Patent and Trademark Office*





US006212079C1

(12) **EX PARTE REEXAMINATION CERTIFICATE** (6800th)  
**United States Patent**  
**Balakrishnan et al.**

(10) Number: **US 6,212,079 C1**  
 (45) Certificate Issued: **May 5, 2009**

(54) **METHOD AND APPARATUS FOR IMPROVING EFFICIENCY IN A SWITCHING REGULATOR AT LIGHT LOADS**

(75) Inventors: **Balu Balakrishnan**, Saratoga, CA (US);  
**Alex B. Djanguerian**, Saratoga, CA (US)

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(73) Assignee: **Power Integrations, Inc.**, Sunnyvale, CA (US)

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No. 90/007,771, Oct. 21, 2005

No. 90/008,376, Dec. 14, 2006

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EP 0 583 038 A1 2/1994  
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(51) **Int. Cl.**  
**H02M 3/335** (2006.01)  
**G05F 1/56** (2006.01)

Primary Examiner—My-Trang Ton

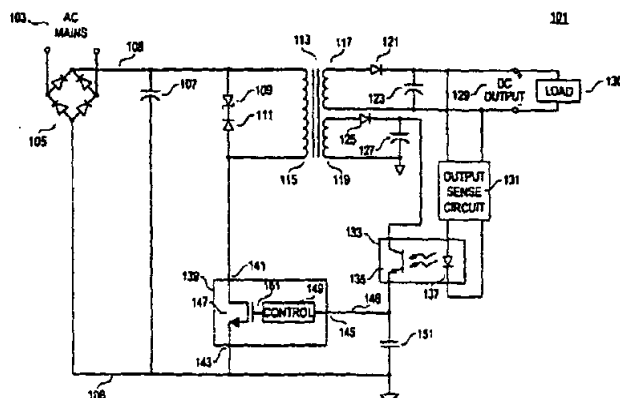
(52) **U.S. Cl.** ..... **363/21; 363/97; 323/284**  
 (58) **Field of Classification Search** ..... None  
 See application file for complete search history.

(57) **ABSTRACT**

A switching regulator that operates at a frequency for a first range of feedback signal values and at a variable frequency without skipping cycles for a second range of feedback signal values. In one embodiment, a switching regulator for a switched mode power supply includes a power switch coupled between drain and source terminals of the switching regulator, which are to be coupled to control the delivery of power to an output of a power supply. A control terminal of the switching regulator is to be coupled to an output of the power supply. The switching regulator includes a control circuit coupled to the control terminal and generates a feedback signal that is responsive to the output of the power supply. The control circuit also generates a drive signal that is coupled to control the switching of the power switch. The control circuit generates the drive signal responsive to the feedback signal. The drive signal has a fixed frequency for a first range of feedback signal values and at a variable frequency without skipping cycles for a second range of feedback signal values.

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1  
**EX PARTE  
REEXAMINATION CERTIFICATE  
ISSUED UNDER 35 U.S.C. 307**

THE PATENT IS HEREBY AMENDED AS  
INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in *italics* indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims 1 and 17 are determined to be patentable as amended.

Claims 2-3, 6, 9, 18 and 19, dependent on an amended claim, are determined to be patentable.

New claims 30-52 are added and determined to be patentable.

Claims 4, 5, 7, 8 10-16 and 20-29 were not reexamined.

1. A switching regulator, comprising:

a power switch coupled between first and second terminals, the first terminal to be coupled to an energy transfer element of a power supply and the second terminal to be coupled to a supply rail of the power supply;

a control circuit coupled to a third terminal and the power switch, the third terminal to be coupled to an output of the power supply, the control circuit coupled to generate a feedback signal responsive to the output of the power supply, the control circuit coupled to switch the power switch in response to the feedback signal[.]; and  
*an oscillator circuit included in the control circuit for controlling both a switching frequency and a maximum duty cycle of the power switch,*

*wherein the control circuit is coupled to switch the power switch at a fixed switching frequency for a first range of feedback signal values when the output of the power supply is in regulation, and wherein the control circuit is coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values when the output of the power supply is in regulation.*

17. A method for regulating a power supply, comprising:  
switching with a drive signal a power switch coupled to an energy transfer element of the power supply to control power delivered to an output of the power supply;  
generating a feedback signal in response to the output of the power supply;

*maintaining a frequency of the drive signal at a fixed frequency for a first range of feedback signal values [and] when the output of the power supply is in regulation;*

*varying the frequency of the drive signal without skipping cycles in response to the feedback signal for a second range of feedback signal values when the power supply output is in regulation; and*

*controlling both the frequency of the drive signal and a maximum duty cycle of the power switch with an oscillator circuit of a controller of the power supply.*

30. The switching regulator of claim 1 wherein a lowest switching frequency of the switching regulator is above a human audible frequency range.

31. A switching regulator, comprising:

a power switch coupled between first and second terminals, the first terminal to be coupled to an energy transfer element of a power supply and the second terminal to be coupled to a supply rail of the power supply; and

a control circuit coupled to a third terminal and the power switch, the third terminal to be coupled to an output of the power supply, the control circuit coupled to generate a feedback signal responsive to the output of the power supply, the control circuit coupled to switch the power switch in response to the feedback signal, the control circuit coupled to switch the power switch at a fixed switching frequency for a first range of feedback signal values, the control circuit coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values, wherein the control circuit comprises:

a feedback signal circuit coupled to the third terminal, the feedback signal circuit coupled to generate the feedback signal; and

a pulse width modulator circuit coupled to switch the power switch in response to the feedback signal,

*wherein the first and second ranges of the feedback signal correspond to first and second ranges of on-time values of a drive signal generated by the pulse width modulator circuit to switch the power switch.*

32. The switching regulator of claim 31 wherein the first and second ranges of the feedback signal further correspond to first and second ranges of duty cycle percentage values of the drive signal generated by the pulse width modulator circuit to switch the power switch.

33. The switching regulator of claim 31 wherein a lowest switching frequency of the switching regulator is above a human audible frequency range.

34. A switching regulator, comprising:

a power switch coupled between first and second terminals, the first terminal to be coupled to an energy transfer element of a power supply and the second terminal to be coupled to a supply rail of the power supply; and

a control circuit coupled to a third terminal and the power switch, the third terminal to be coupled to an output of the power supply, the control circuit coupled to generate a feedback signal responsive to the output of the power supply, the control circuit coupled to switch the power switch in response to the feedback signal, the control circuit coupled to switch the power switch at a fixed switching frequency for a first range of feedback signal values, the control circuit coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values, wherein the control circuit comprises:

a feedback signal circuit coupled to the third terminal, the feedback signal circuit coupled to generate the feedback signal; and

a pulse width modulator circuit coupled to switch the power switch in response to the feedback signal, and wherein on-time and off-time values of a drive signal generated by the pulse width modulator circuit to switch the power switch vary simultaneously as a



function of a level of a load coupled to the output of the power supply to vary the switching frequency of the power switch without skipping cycles for the second range of feedback signal values.

35. The switching regulator of claim 34 wherein the off-time value of the drive signal is varied as a function of the on-time value and a first on-time value of the drive signal, the first on-time value of the drive signal corresponding to an on-time of the drive signal at a boundary between the first and second ranges of feedback signal values.

36. The switching regulator of claim 34 wherein the switching frequency of the power switch is reduced without skipping cycles to a minimum frequency when a duty cycle percentage value of the drive signal generated by the pulse width modulator circuit to switch the power switch is substantially equal to zero percent.

37. The switching regulator of claim 34 wherein a lowest switching frequency of the switching regulator is above a human audible frequency range.

38. A switching regulator, comprising:

a power switch coupled between first and second terminals, the first terminal to be coupled to an energy transfer element of a power supply and the second terminal to be coupled to a supply rail of the power supply; and

a control circuit coupled to a third terminal and the power switch, the third terminal to be coupled to an output of the power supply, the control circuit coupled to generate a feedback signal responsive to the output of the power supply, the control circuit coupled to switch the power switch in response to the feedback signal, the control circuit coupled to switch the power switch at a fixed switching frequency for a first range of feedback signal values, the control circuit coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values, wherein the first and second ranges of the feedback signal correspond to first and second ranges of on-time values of a drive signal generated by the control circuit to switch the power switch.

39. The switching regulator of claim 38 wherein the first and second ranges of the feedback signal further correspond to first and second ranges of duty cycle percentage values of the drive signal generated by the control circuit to switch the power switch.

40. The switching regulator of claim 38 wherein the control circuit comprises an oscillator circuit for controlling both the switching frequency and a maximum duty cycle of the power switch.

41. The switching regulator of claim 38 wherein a lowest switching frequency of the switching regulator is above a human audible frequency range.

42. A switching regulator, comprising:

a power switch coupled between first and second terminals, the first terminal to be coupled to an energy transfer element of a power supply and the second terminal to be coupled to a supply rail of the power supply; and

a control circuit coupled to a third terminal and the power switch, the third terminal to be coupled to an output of the power supply, the control circuit coupled to generate a feedback signal responsive to the output of the power supply, the control circuit coupled to switch the power switch in response to the feedback signal, the control circuit coupled to switch the power switch at a fixed switching frequency for a first range of feedback

signal values, the control circuit coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values, wherein on-time and off-time values of a drive signal generated by the control circuit to switch the power switch vary simultaneously as a function of the feedback signal in the second range of feedback signal values.

43. The switching regulator of claim 42 wherein the off-time value of the drive signal is varied as a function of the on-time value and a first on-time value of the drive signal, the first on-time value of the drive signal corresponding to an on-time of the drive signal at a boundary between the first and second ranges of feedback signal values.

44. The switching regulator of claim 42 wherein the switching frequency of the power switch is reduced without skipping cycles to a minimum frequency when a duty cycle percentage value of the drive signal generated by the control circuit to switch the power switch is substantially equal to zero percent.

45. The switching regulator of claim 42 wherein the control circuit comprises an oscillator circuit for controlling both the switching frequency and a maximum duty cycle of the power switch.

46. The switching regulator of claim 42 wherein a lowest switching frequency of the switching regulator is above a human audible frequency range.

47. A switching regulator, comprising:

a power switch coupled between first and second terminals, the first terminal to be coupled to an energy transfer element of a power supply and the second terminal to be coupled to a supply rail of the power supply;

a control circuit coupled to a third terminal and the power switch, the third terminal to be coupled to an output of the power supply, the control circuit coupled to generate a feedback signal responsive to the output of the power supply, the control circuit coupled to switch the power switch in response to the feedback signal; and

an oscillator circuit included in the control circuit for controlling both a switching frequency and an on-time of the power switch,

wherein the control circuit is coupled to switch the power switch at a fixed switching frequency for a first range of feedback signal values when the output of the power supply is in regulation, and wherein the control circuit is coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values when the output of the power supply is in regulation.

48. The switching regulator of claim 47 wherein a lowest switching frequency of the switching regulator is above a human audible frequency range.

49. The switching regulator of claim 47 wherein the first and second ranges of the feedback signal correspond to first and second ranges of on-time values of a drive signal generated by the control circuit to switch the power switch.

50. A switching regulator, comprising:

a single power switch to be coupled between first and second terminals, the first terminal to be coupled to an energy transfer element of a power supply and the second terminal to be coupled to a supply rail of the power supply;

a control circuit coupled to a third terminal of the switching regulator and to the single power switch, the third

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terminal to be coupled to an output of the power supply, the control circuit coupled to generate a feedback signal responsive to the output of the power supply, the control circuit coupled to switch the power switch in response to the feedback signal, the control circuit coupled to switch the power switch at a fixed switching frequency for a first range of feedback signal values when the output of the power supply is in regulation, the control circuit coupled to vary a switching frequency of the power switch without skipping cycles in response to the feedback signal for a second range of feedback signal values when the power supply output is in regulation.

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wherein the control circuit comprises an oscillator circuit for controlling both the switching frequency and a maximum duty cycle of the power switch.

51. The switching regulator of claim 50 wherein a lowest switching frequency of the switching regulator is above a human audible frequency range.

52. The switching regulator of claim 50 wherein the first and second ranges of the feedback signal correspond to first and second ranges of on-time values of a drive signal generated by the control circuit to switch the power switch.

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